CS302 Quiz-1 BY Attiq Kundi

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CORRECT MCSQ

AND Many MoRe

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1. **In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.**

1. True
2. False

2. **Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using_____.**

1. Shift Registers
2. Circular Buffers
3. Ring Buffers
4. Reduce Registers

`

3. **The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to_____location(s) using a single address.**

1. One
2. Two
3. Three
4. Four

4. **When the transmission line is idle in an asynchronous transmission**

1. It is set to logic low
2. It is set to logic high
3. It remains in previous state
4. State of transmission line is not used to start transmission

5. **A multiplexer with a register circuit converts**

1. Serial data to parallel
2. Parallel data to serial
3. Serial data to serial
4. Parallel data to parallel

6. **_____is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.**

    1. Combinational Input/Output
    2. Combinational Output 3.

    Combinational Input

    4. Programmable polarity

7. **The terminal count of a 4-bit binary counter in the UP mode is ____.**

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1. 1100
2. 0011
3. 1111
4. 0000

8. A SOP expression can be implemented by an_____combination of gates.

1. OR-XOR
2. AND-NAND
3. AND-OR
4. XOR-NOR

9. The n flip-flops store_____states.

1. 1
2. 2^n
3. 0
4. 2^(n+1)

10. The AND Gate performs a logical_____function.

1. Addition
2. Substraction
3. Multiplication
4. Division

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12. **Implementation of Latch is required almost_____transistor.**

1. Two
2. Four
3. Six
4. Eight

13. **For a Standard SOP expression, a_____is placed in the cell corresponding to the product term (Minterm) present in the expression.**

1. 0
2. 1
3. x (don't care condition)
4. Any of given option depending on SOP term

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14. **Demorgan's two theorems prove the equivalency of the NAND and ___gates and the NOR and_____gates respectively.**

1. Negative-OR, Negative-AND
2. Negative-AND, Positive-OR
3. Positive-OR, Negative-AND
4. Positive-OR, Positive-AND

15. **The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as inputs.**

1. Sequential
2. Asynchronous 3.
4. Combinational Synchronous

16. **The Test Vector definition defines the test vectors for all the three counter inputs and counter output/outputs.**

1. One
2. Two
3. Three
4. Four

17. **Select the mode of programming in which GAL16V8 can be programmed:**

1. Simple Mode
2. Complex Mode
3. Registered Mode
4. All of the given

18. **If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a_____.**

1. 0
2. 1

19. **The ROM used by a computer is relatively_____as it stores few byres of code used to Boot the Computer system on power up.**

1. Small
2. Large
3. Heavy
4. High

20. **In NAND based S-R latch, output of each____gate is connected to the input of the other gate.**

1. NOR, NAND
2. NAND, NOR
3. NOR, NOR
4. NAND, NAND

21. **The outputs of SR latches in elevator state machine are feed back to the____gate array for connection to the D-flipflops.**

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1. NOT
2. AND
3. OR
4. XOR

22. The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the_____can be pressed at any time either on the first floor or the second floor in elevator.

1. REQ0
2. OPEN
3. REQ1
4. FLOOR1

23. The CONSTATE.CLK = Clock is used to indicate that the_____state variables change on a clock transition.

1. CONSTATE
2. FLOOR
3. MOTION
4. OPEN

24. A NOR based S-R latch is implemented using_____gates instead of gates.

1. XOR, NAND
2. NOR, XOR
3. NOR, NAND
4. OR, XOR

25. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting__.

1. Q output of all flip-flops to clock input of next flip-flops
2. Q' output of all flip-flops to clock input of next flip-flops
3. Q output of all flip-flops to J input of next flip-flops
4. Q' output of all flip-flops to K input of next flip-flops

26. Consider the sum of weight method for converting decimal into binary value,_____is the highest weight for 411.

1. 64
2. 128
3. 256
4. 512

27. The 64-cell array organized as 8 x 8 cell array is considered

1. as an 64 byte memory
2. as a 16 byte memory 3. as an 8 byte memory

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4. as an 4 byte memory

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28. **Implementation of the FIFO buffer in_____is usually takes the form of a circular buffer.**

1. RAM
2. ROM
3. PPROM
4. Flash Memory

29. **If two numbers in BCD representation generate an invalid BCD number then the binary is added to the result.**

33. **The FAST Model Page Access allows_____memory read and access times when reading successive data values stored in consecutive locations on the same row.**

1. Slow 2.

Faster

3. Medium
4. Modern

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34. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

1. True
2. False

35. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in
___when Distributed refresh is used.

1. 4.8 microsec
2. 5.9 microsec
3. 7.8 microsec
4. 5.5 microsec

36. The output of a NAND gate is_____when all the inputs are one.

1. Zero

41. Divide-by-32 counter can be achieved by using

1. Flip-Flop and DIV 10
2. Flip-Flop and DIV 16 3.

Flip-Flop and DIV 32

4. DIV 16 and DIV 32

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42. **If the number of samples that are collected is reduced by half, the reconstructed signal will be_____from/to the original.**

1. Different
2. Same
3. Equal
4. Opposite

43. **The Transition table is very similar to the_____table.**

1. Truth
2. State
3. Transition
4. None of the given

44. **GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a_____with a_____.**

1. column, row
2. row, column
3. column, column
4. row, row

45. **UVERPROM is stands for**

1. Ultra-Variant
2. Ultra-Vibrant
3. Ultra-Voilet
4. Ultra-Visible

46. **8-bit parallel data can be converted into serial data by using _____ multiplexer.**

1. 4-to-2
2. 8-to-1
3. 4-to-4
4. 8-to-4

47. **Implementing the Adjacent 1s detector circuit directly from the function table based on the SOPform requires_____gates for the 8 product terms (minterms) with an 8-input OR gate.**

1. 8 OR
2. 8 AND
3. 8 XOR
4. 8 NOR

48. **Why demultiplexer is called a data distributor?**

1. The input will be distributed to one of the outputs
2. The input will be selected for the output
3. The output will be distributed to one of the inputs 4. Single input to Single Output

49. **A 3-variable karnaugh map has**

1. eight cells
2. three cells

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50. **Flash memory Operation are classified into _____ operation.**

1. Two
2. Three
3. Four
4. Five

different

51. **The Static Ram (SRAM) is non-volatile and is not a_____density memory as a latch is required to store a single bit of information.**

1. Low
2. High
3. Medium
4. Hot

52. **You have to choose suitable option when your timer will reset by considering this given code:**

```
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);
```

1. NSY2 or EWY2
2. NSSR or TMRST
3. EWSR or NSRED
4. EWRed or EWYel

53. **Which of the following is a volatile memory?**

1. PROM
2. DRAM
3. EPROM
4. EEPROM

54. **The ABEL Input file can use a_____instead of the equation to specify the Boolean expressions.**

1. Truth Table
2. State Diagram
3. Karnaugh Map
4. Logic Circuit

55. **The domain of the expression AB'CD + AB' + C'D + B is**

1. A and D
2. B only
3. A, B, C and D
4. None of the given

56. **The maximum value, represented by a single hexadecimal digit is ____.**

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1. "E"

2. "F"

3. "G"

4. "H"

57. PALs tend to execute_____logic.

1. SPD

2. SOP

3. SAC

4. SAP

58. Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be_____.

1. Zero

2. One

3. Undefined

4. No output as input is invalid

59. PLDs have In-System Programming (ISP) capability that allows the ___ to be programmed after they have been installed on a circuit board.

1. PLAs

2. PALs

3. PLDs

4. EPROM

60. _____ Counters as the name indicates are not triggered simultaneously.

1. Asynchronous

2. Synchronous

3. Positive-Edge triggered

4. Negative-Edge triggered

61. Adding two octal numbers "36" and "71" result in_____.

1. 213

2. 123

3. 127

4. 345

62. In DRAM read cycle R /W- signal is activated to read data which is made available on the data line.

1. D(IN) 2.

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D(OUT)

3. D(AB)

4. D(INT)

63. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack ____.

1. Bottom

2. Top

3. Down

4. Vertex

64. For a down counter that counts from (111 to 000), if current state is "101" the next state will be_____.

1. 111

2. 110

3. 010

4. None of the given

65. Which one flip-flop has an invalid output state?

1. T

2. JK

3. SR

4. D

66. Two signals_____and_____provide the timing inputs to the State Machine.

1. NSSR and EWSR

2. LTIME and STIME

3. PTIME and QTIME

4. NSGrn and NSYel

67. The Adjacent 1s Detector accepts 4-bit inputs. If_____adjacents 1s are detected in the input, the output is set to high.

1

68. Canonical form is a unique way of representing_____.

SOP

69. Subtractors also have output to check if 1 has been_____.

1. Primed

2. Shifted

3. Complemented

4. Borrowed

70. The_____input overrides the_____input.

1. Asynchronous, synchronous

2. Synchronous, asynchronous

3. Preset input (PRE), Clear input (CLR)

4. Clear input (CLR), Preset input (PRE)

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71. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

1. $\overline{CS}$ 2. $\overline{WE}$
3. W
4. OE

72. The NOR logic gate is the same as the operation of the_____gate with an inverter connected to the output.

1. AND

Combinational Logic is used for combinational circuits, where as Registered Logic is based

on ----------circuits

Sequential circuits 192(Page)

A standard interface for programming the In-System PLD consists of

4-wire 194(Page)

The 4-bit ALU (74XX381) only has three function select inputs allowing only different _____ arithmetic and logic functions.

8 147(Page)

Which of the following is the MSI version of the Look-Ahead Carry Generator, which provides identical inputs and outputs except for the C4 output?

74XX182 151(Page)

The PROM consists of a fixed non-programmable_____Gate array configured as a decoder.

AND 182(Page)

Each Octal Number digit can represent a_____Binary Number

3-bit 31(Page)

The simplified expressions using either of the two K-maps are ----------?

Identical 89(Page)

The_____gate and_____gate implementation connected at the B input of the 4-bit Adder

AND and OR 146(Page)

In 16-Input Multiplexer, the four outputs are connected together through a 4-input gate.? _____

OR 171(Page)

___is invalid number of cells in a single group formed by the adjacent cells in K-map

12 Google

XOR is an abbreviation of_____.

Exclusively-ORGoogle

For a 3-to-8 decoder how many 2-to-4 decoders will be required?

Decoders Google

The expression F=A.B.C describes the operation of three bits_____Gate.

0RGoogle

How many sets of AND-OR based circuit are used to allow complemented and un-complemented B input to be applied at the B inputs of the two 4-bit Adders? **Tw0**

146(Page)

The product terms in Standard SOP are called_____

Minterms 85(Page)

"The complement of a product of variables is equal to the sum of the complements of the variables." is known as:

Demorgan's First Theorem 74(Page)

Basic function of a Comparator is to_____two binary quantities.

Compare 153(Page)

The_____output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

Programmed Polarity 186(Page)

Power consumption in TTL is_____as compared to CMOS.

Higher than 61(Page)

Enable input of the decoder when set to 1 disables the decoder and the multiplexers.

G 171(Page)

A Karnaugh Map is organized in the form of a(an)_____.

Array 89(Page)

Gate is used in circuits to generate the 1's Complement of a number by inverting all its bits.

NOT 44(Page)

The OR Gate performs a Boolean_____function

Addition

The expression F=A+B+C

OR

In Caveman number system the value "2" is represented by symbol _____

> 11(Page)

A SOP expression having a domain of 3 variables will have a truth table having ___combinations of inputs and corresponding output values.

4

A standard SOP form has_____terms that have all the variables in the domain of the expression.

Product

Caveman number system is Base_____number

5

74ALS stands for _____

Advanced Low-Power Schottky TTL

The ANSI/EEE Standard 754 defines a_____Single-Precision Floating Pointing format for binary numbers.

32-bit

The output of an AND gate is one when

All of the input are one

Excess-8 code assigns_____to "-8"

0000

_ is invalid number of cells in a single group formed by the adjacent cells in K- map

12

The cell marked 6 in 4-variable K-Map represent minterm 6 or the maxterm 6 having the following binary value of variables A, B, C and D.

A=1, B=0, C=0, D=1

A=0, B=1, C=1, D=0

The hexadecimal value “FD” is equivalent to binary value _____

11111101

The Extended ASCII Code (American Standard Code for Information Interchange) is a_____code

7bit

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

True

The 4-bit 2’s complement representation of “-7” is _____

1001 **23(Page)**

The ABEL symbol for “OR” operation is

#

A standard SOP form has_____terms that have all the variables in the domain of the expression.

Sum **85(page**

How many data select lines are required for selecting eight inputs?

3

If two adjacent 1s are detected in the input, the output is set to high. input combin ations will be

0011

The 4-variable Karnaugh Map (K-Map) has_____rows and_____colums

4,4

The boolean expression A + B' + C is

a sum term

the boolean expression AB'CD'is
a product term

Don’t care conditions are marked as_____in the output column of the function table

X

An example of SOP expression is

both (a) and (b)

For a Standard SOP expression, a_____is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Multiplexers are also known as_____.

Data Selectors

Sum term (Max term) is implemented using_____gates

OR

The number “1259” may belong to_____number system.

Binary or Hexadecimal system

If two numbers in BCD representation generate an invalid BCD number then the binary_____is added to the result

1111

“1101” in signed representation is equivalent to _____

13

TTL based devices work with a dc supply of_____Volts

+5

In decimal value “275” the weight of the digit “7” is _____

100

The decimal “10” will have an octal equivalent _____

12

Caveman number system is Base_____number system 5

How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?

1 bits

The total amount of memory is depends upon _____
The size of the address bus of the microprocessor

_____can be determined the Instability condition. logic diagram

If we add an inverter at the output of AND gate, what function is produced? NAND

Which is also known as coincidence detector? AND gate

Transition table include _____
squares

For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?

Truth table

Stack is an acronym for _____
LIFO memory

When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called _____

Race condition

positive OR gate is also a negative AND gate

Time delay device is memory element of_____
asynchronous circuits

Boolean algebra is also called
A- arithmetic algebra
B- switching algebra
Both A & B

Boolean function must be brought into_____To perform product of max terms

OR terms

The binary number 10101 is equivalent to the decimal number_____.

21

The domain of expression ABCD + AB + CD + B is— B only

The Boolean expression A BC D is— Sum term

The universal gate is_____.

NAND gate

According to boolean algebra absorption law, which of the following is correct?

xy+y=x

A Boolean function may be transformed into logical diagram

The inverter is _____

NOT gate

The resulting circuit of a NAND gate are connected together is_____

NOT gate

x*y = y*x is the
identity element

Minterms are also called
standard product

OR gate and_____will form The NOR gate?

NOT gate

The NAND gate is AND gate followed by ……
NOT gate

Max terms are also called_____.
standard sum

In Boolean algebra Multiplicative inverse is a

By the repeated use of_____Digital circuit can be made

NAND gates

The only function of NOT gate is_____of the following.
Invert input signal

Boolean algebra is defined as a set of_____.
two values

First operator precedence for evaluating Boolean expressions is Parenthesis

The output is_____When an input signal 1 is applied to a NOT gate 0

The bar sign (-) indicates_____In Boolean algebra?
NOT operation

The value of n is_____when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.

10

2's complement of binary number 0101 is _____
1011

An OR gate has 4 inputs. The output is ……. When One input is high and the other three are low.

High

To convert BCD to seven segments_____device is used.
Decoder

Decimal number 10 is equal to binary number_____.
1010

In 2's complement representation the number 11100101 represents the decimal number_____.

-27

BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are_____.

All

A decade counter skips_____.
binary states 1010 to 1111

___Number of States A ring counter with 5 flip flops will have? 5

Positive edge-triggered flip-flop changes its state when _____
Low-to-high transition of clock

If S=1 and R=1, for negative edge triggered flip-flop then Q(t+1) = _____
Invalid

A 5-variable karnaugh map has

Thirty two cells

8-bit parallel data can be converted into serial data by using_____multiplexer
8-to-1 ok **175(page)**

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

Divide-by-32 counter can be acheived by using Flip-Flop
and DIV 16

The Synchronous counters are also known as Ripple Counters: False ok

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW **235(Page)**

Which of the number is not a representative of hexadecimal system?

"1001" correct

High level Noise Margins (VNH) of CMOS 5 volt series circuits is _ 0.9 V
correct

To get the answer "1" in Boolean addition of three variables, _____

One of the variables must be 1 correct

The 3-variable Karnaugh Map (K-Map) has_____cells for min or max terms 8
correct

___is invalid number of cells in a single group formed by the adjacent cells in K-map
2 correct

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be __

Zero

The Binary number 1011.101 has an Integer part represented by_____and a fraction part_____separated by a decimal point.

1011, 101

1011+101 = _
10000

Adding two octal numbers "36" and "71" result in _____
127

The first Least Most digit in decimal number system has Has position
0 and weight equal to 1

Sum term (Max term) is implemented using_____gates
OR

The OR Gate performs a Boolean_____function
Add 42

Adding two octal numbers "36" and "71" result in _____
127

NOR Gate can be used to perform the operation of AND, OR and NOT Gate TRUE

The three fundamental gates are _____
NOT, OR, AND

A SOP expression having a domain of 3 variables will have a truth table having
___combinations of inputs and corresponding output values. 4
87

Which of the following is the octal equivalent of 28 decimal number? 34

The maximum decimal number that can be represented using the 64-bit unsigned representation is_____.

(2^64)-1

In a 4-variable K-map, a 2-variable product term is produced by a 4-cell group of 1s

For a Standard SOP expression, a_____is placed in the cell corresponding to the product term present in the expression.

1

The_____input select/deselects both the decoders simultaneously. Enable

NAND and_____gates are known as Universal Gates. NOR

The declaration section of ABEL generally includes the device declaration, ___declarations and set declarations. Pin

An SOP expression having a domain of 2 variables will have a truth table having ___combinations of inputs and corresponding output values. 4

In the 32-bit Single Precision Floating formation, the exponent value ___is reserved to represent 0 exponents. 0

CMOS technology is characterized by low power dissipation with _____ switching speeds.

Slow

The complement of a variable is always The inverse of the variable

A (B + C) = A.B + A.C is the expression of_____. Distributive Law

If the number 2025 is represented in floating point, then exponent is ___.3

Excess-8 code of -6 is_____. 0010

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is___to the range of values that are to be represented. Proportional

Suppose we want to transmit the data "10001101" and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to the data will be_____ Both "0" and "1" can be used

The carry propagation delay problem in parallel binary adder can be solved by ___. Using two full adders

Two 2-input, 4-bit mulitplexers 74X157 can be connected to implement a ___multiplexer. 2-input, 8-bit

The octal equivalent of the following binary number is _____

117

A' is written is ABEL as_____.
!A

Which of the following is the hexadecimal equivalent of 28? 1C

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is _ 0.9 V

Adjacent 1s detector circuit will have active high output for the input. 0011 123

Modern information techniques are relying more on_____transmission.
Digital

The_____select input(s) of the two 4-input multiplexers are common in Dual 4- input multiplexer.
Two

How many data select lines are required for selecting eight inputs? 3

Select the mode of programming in which GAL 16V8 cam be programmed. All of the given option

___has the fastest switching speed and low power requirement. Advanced low power Schottky

The PLA can be programmed to give an output of constant_____or_____.
0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called___of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at_____of the clock signal.
One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flip using NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is

1111

___is said to occur when multiple internal variables change due to change in one input variable
Race condition

The Synchronous counters are also known as Ripple Counters: False

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the ____

Set-up time

The n flip-flops store_____states
2^n

When the_____Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of _____
1,2

A positive edge-trigged flip-flop changes its state when _____
Low-to-high transition of clock

A decade counter is _____
Mod-10 counter

The look-ahead carry circuits_____
Reduce propagation delay

If two numbers in BCD representation generate an invalid BCD number then the binary___is added to the result

0110

Both the multiplexers are selected simultaneously when_____is set to logic ___in 2-inputs, 8-bit Multiplexer. G, Low

Function labels required to represent the input/output combinations for each segment in 7-segment display
7

Multiplexers are also known as _____
Data selectors

Cin is part of ____ Adder.
Full

The look-ahead carry circuits_____
Reduce propagation delay

The PLA can be programmed to give and output of constant_____or_____
0, 1

Which of the following gates has the outputs 1 if and only if at last one input is 1? OR

A sop expression can be implemented by on_____combination of gates.
AND-OR

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through_____ALU units in 16-bit ALU.
Four **150(Page)**

Digital circuits operates with_____voltage value(s) 2

The_____is the slowest and consumes more power.
Standard TTL 61

The between expression X-AB+CD represents Two
ANDs ORed together

Which one of the following is NOT a valid rule of Boolean Algebra? A=A' 73

A 5-Variable Karnaugh map has
Thirty two cells

___is invalid number of cells in a single group formed by the adjacent cells K- map
12

In 32-bit Single –Precision floating point format representation the range of exponent value is from_____to _____

+127 to -126

___has the fastest switching speed and low power requirements Advanced low power Schottky

Which of the following is a volatile memory? DRAM

___is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.
Combinational Input

The AND Gate performs a logical_____function.
multiplication **40(Page)**

The Adjacent 1s Detector accepts 4-bit inputs. If_____adjacent 1s are detected in the input, the output is set to high.

2 **123(Page)**

In 16-input multiplexer, the decoder inputs and enable one out of the four multiplexers.

C and D **171(Page)**

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

The FAST Model Page Access allows_____memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a_____with a_____.

row, column

Which of the following Output Equations determines the output of the State Machine?

MAX = Q0Q1EN

The maximum value, represented by a single hexadecimal digit is_____.

"F"

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a_____.

1

The Static Ram (SRAM) is non-volatile and is not a_____density memory as a latch is required to store a single bit of information.

High

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and_____gates respectively.

Negative-OR, Negative-AND

Two signals_____and_____provide the timing inputs to the State Machine.

PTIME and QTIME

The 74HC163 is a 4-bit Synchronous counter, it has_____data output pins. 4

PLDs have In-System Programming (ISP) capability that allows the____to be programmed after they have been installed on a circuit board.

PLDs

The CONSTATE.CLK = Clock is used to indicate that the_____state variables change on a clock transition.

CONSTATE

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using_____.

Shift Registers

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as ___inputs.

Synchronous

For a down counter that counts from (111 to 000), if current state is "101" the next state will be_____.

None of the given

The_____gate and_____gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to_____location(s) using a single address.

Four

In NAND based S-R latch, output of each_____gate is connected to the input of the other_____gate.

NAND, NAND

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires_____gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

The_____input overrides the_____input.

Asynchronous, synchronous

A SOP expression can be implemented by an_____combination of gates.

AND-OR

The 64-cell array organized as 8 x 8 cell array is considered as an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is_____.

1100

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting_____.

Q output of all flip-flops to clock input of next flip-flops

Memory is arranged in_____.

Two-dimensional manner

If two numbers in BCD representation generate an invalid BCD number then the binary_____is added to the result.

1001

Subtractors also have output to check if 1 has been_____.

Primed

The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

Three

A multiplexer with a register circuit converts Parallel data to serial

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The n flip-flops store_____states.

2^n

The S-R latch has two inputs, therefore_____different combinations of inputs can be applied to control the operation of the S-R latch.

four

Why demultiplexer is called a data distributor? Single input to Single Output

When the transmission line is idle in an asynchronous transmission It is set to logic high

UVERPROM is stands for
Ultra-Voilet

In memory write cycle, the time for which the WE signal remains active is known as the___.
Write pulse width

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

AND

PALs tend to execute_____logic.
SOP

The ROM used by a computer is relatively_____as it stores few buyers of code used to Boot the Computer system on power up.

Small

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

$\overline{WE}$

You have to choose suitable option when your timer will reset by considering this given code:

TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2); NSY2 or EWY2

A NOR based S-R latch is implemented using_____gates instead of ___gates. NOR,
NAND

Implementation of Latch is required almost_____transistor.
Six

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in_____when Distributed refresh is used.

7.8 microsec

The NOR logic gate is the same as the operation of the_____gate with an inverter connected to the output.

NAND

Select the mode of programming in which GAL16V8 can be programmed: All of the given

Divide-by-32 counter can be achieved by using Flip-Flop and DIV 32

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the ___can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be_____.

One

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

Adding two octal numbers "36" and "71" result in_____.

127

The ABEL Input file can use a_____instead of the equation to specify the Boolean expressions.

Truth Table

The domain of the expression AB'CD + AB' + C'D + B is A, B, C and D

If the number of samples that are collected is reduced by half, the reconstructed signal will be_____from/to the original.

Different 1

In DRAM read cycle R /W^{-} signal is activated to read data which is made available on the_____data line.

D(OUT)

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Implementation of the FIFO buffer in_____is usually takes the form of a circular buffer.

RAM

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack_____.

Top

Which one flip-flop has an invalid output state? SR

The output of a NAND gate is_____when all the inputs are one.
1

The Transition table is very similar to the_____table.
State

Consider the sum of weight method for converting decimal into binary value,
___is the highest weight for 411.
256

Canonical form is a unique way of representing_____.
SOP

___Counters as the name indicates are not triggered simultaneously. Synchronous

Cin is part of_____Adder.
Full

Flash memories Operation are classified into_____different operation.
Two

A Product term is 0 when_____
Any one literal is 0

In 8-inpit multiplexer, the two outputs are connected through a/an _____ gate.
OR

___Device dissipate varying amount of power depending upon the frequency of operation.
CMOS

Boolean Addition operation is performed by a(an) ____ gate.
OR

A SOP expression can be implemented by an_____combination of gates.
AND-OR

The maximum decimal number that can be represented using the 64-bit unsigned representation is_____.

(2^64)-1

In 16-bit ALU, The G output is activated if the 4-bi unit generate a Carry _____ irrespective of Carry___.

Out,In 150

A standard POS from has_ters that have all the variables in the domain of the expression.

Sum

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles__.

Lower priority inputs

Which of the following is the example of comparater? XNOR

IN CMOS 5 Volt series, Input voltage of Logic high signal (VIH) with a ranges from_____to_____volts.

3,5,5

The Adjacent 1 S Detector accepts 4-bits input. If___adjacent 1S are detected in the input, the output is set to high.

4

DE Morgan's two theorems prove the equivalency of the NAND and____gates and the NOR and gates respectively.

Negative-AND, Negative-OR

Adding two octal numbers "36 and 71" result in_____. 127

Any of the_____forms of the Karnaugh Map can be used to simplify Boolean expressions

2

Quine-McCluskey and K-Map methods are used for_____of Boolean expression.
Simplification 111

The number "1259" may belong to_____number system.
Decimal or Hexadecimal system

The series of TTL chips are characterized by their_____.
Switching Speed only 61

The_____input selects/deselects both the decoders simultaneously.
Enable

All ABEL statements must end with_____.
;

In sequential circuit memory elements are connected with_____.
Clock

In the 32-bit Single Precision Floating Point format, the exponent value_____is reserved to represent infinity exponents.

255

The limitation in implementation of parallel binary address is known as_____.

Carry input

The Gray code is different form the unsigned binary code because_____.
Successive value of Gray code by only one bit

Removing the NOT gate at the output of the NOR gate result in an_.
OR gate 50

Portable devices that run on batteries use__circuit that have low power dissipation.

Integrated

The domain of the expression AB'CD+B is

B only

__is a single input gate
OR

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is _____to the range of values that are to be represented.
Equal

BCD code of 16 is_____.
00010001

To determine the seven expressions for each of the seven outputs in 7-segment display, seven_____variable Karnaugh Maps are used.

3

In Odd parity generator circuit which gate is used to detect parity errors?
XOR

A 3-variable Karnaugh map has
Eight cells

The measurable values generally change over a
Continuous range

___uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.

GAL

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?

1001

The expression_____is an example of Commutative Law for Multiplication.

AB=BA

The look-ahead carry circuits_____

Reduce propagation delay

What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

B'+C'D'+CD

The range of Excess-8 code is from

_____ to _____

+7 to -8

In a K-map simplification method, a group of four adjacent 1,s lead to a term with two literals less than the total number of variables

• Collection by by Attiq Kundi

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