Cs302

Digital Logic Design

Final Term Most Important & Repeated MCQs

Final Term Preparation 2022

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DE multiplexer converts _____ data to _____ data

Select correct option:

- Parallel data, serial data
- Serial data, parallel data (Page 356)
- Encoded data, decoded data
- All of the given options.

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

Select correct option:

- 0
- 1 (Page 230)
- Invalid
- Input is invalid

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

Select correct option:

- 0
- 1
- Invalid (Page 230)
- Input is invalid

Learning With A&I

In asynchronous digital systems all the circuits change their state with respect to a common clock

Select correct option:

- True
- False (Page 245)

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

Select correct option:

- 10 mW
- 25 mW (Page 242)
- 64 mW
- 1024

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

Select correct option:

- 10 Hz
- 50 Hz (Page 298)
- 100 Hz
- 500 Hz

Learning With A&I

Cs302 Final Term Most Important MCQs

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

Select correct option:

- NAND
- AND
- OR
- NOT

The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.

Select correct option:

- Small Page423
- Heavy
- High
- Normal

In _____ outputs depend only on the combination of current state and inputs.

Select correct option:

- Mealy machine (Page 332)
- Moore Machine
- State Reduction table
- State Assignment table

Cin is part of _____ Adder.

Learning With A&I

Select correct option:

- Full
- Half
- Single
- Double

Which one flip-flop has an invalid output state?

Select correct option:

- SR
- T
- JK
- D

Following is standard POS expression

Select correct option:

- True
- False

In the following statement Z PIN 20 ISTYPE „reg.invert";

The keyword "reg.invert" indicates _____

Select correct option:

- An inverted register input
- An inverted register input at pin 20
- Active-high Registered Mode output
- Active-low Registered Mode output (Page 360)

Learning With A&I

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.

Select correct option:

- Set
- Reset
- Latch
- Toggle

In synchronous systems, the exact times at which any output can change state are determined by a signal commonly called the _____.

Select correct option:

- Traffic
- D
- Flip-flop
- Clock

Which is not an example of a truncated modulus?

Select correct option:

- 8
- 9
- 11
- 15

Learning With A&I

The maximum value, represented by a single hexadecimal digit is ____.

Select correct option:

- "F"
- "E"
- "G"
- "H"

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Select correct option:

- Read Only Memory
- Fist In First Out Memory (Page 425)
- Flash Memory
- Fast Page Access Mode Memory

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack __.

Select correct option:

- Top Page422
- Bottom
- Down
- Vertex

Learning With A&I

8-bit parallel data can be converted into serial data by using _____ multiplexer.

Select correct option:

- 8-to-1 Page175
- 8-to-0
- 0-to-8
- 1-to-0

Adding two octal numbers "36" and "71" result in _____.

Select correct option:

- 127
- 213
- 123
- 345

The process of converting the analogue signal into a digital representation (code) is known as _____

Select correct option:

- Strobing
- Amplification
- Quantization (Page 445)
- Digitization

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state Select correct option:

Learning With A&I

Select correct option:

- Ten
- Eight
- Three
- Two Page255

A standard interface for programming the In-System PLD consists of

Select correct option:

- 2 wire,
- 4 wire page no 194
- 8 wire,
- 16 wire

In designing any synchronous counter a modulus number is used which determine the number of…… used in a counter…..

Select correct option:

- Registers
- Flip Flops
- Counters
- Latches

The alternate solution for a multiplexer and a register circuit is _____

Select correct option:

- Parallel in / Serial out shift register (Page 356)
- Serial in / Parallel out shift register
- Parallel in / Parallel out shift register
- Serial in / Serial Out shift register

Learning With A&I

A positive edge-triggered flip-flop changes its state when _.

Select correct option:

- Enable input (EN) is set
- Preset input (PRE) is set
- Low-to-high transition of clock
- High-to-low transition of clock

The asynchronous inputs are normally labeled _____ and _____, and are normally active_____ inputs.

Select correct option:

- PRE, CLR, LOW
- ON, OFF, HIGH
- START, STOP, LOW
- SET, RESET, HIGH

A Nibble consists of _____ bits

Select correct option:

- 1
- 2
- 3
- 4 Page394

Learning With A&I

Smallest unit of binary data is a _____

Select correct option:

- Bit (Page 394)
- Nibble
- Byte
- Word

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

Select correct option:

- 0
- 1 Page417
- 2
- 3

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state.

On the next clock pulse, to what state does the counter go?

Select correct option:

- 1001
- 1011
- 0011
- 1100

Learning With A&I

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

Select correct option:

- 25 mW Page242
- 10 mW
- 64 mW
- 1024 mW

In _____ outputs depend only on the current state.

Select correct option:

- Mealy machine
- Moore Machine (Page 332)
- State Reduction table
- State Assignment table

In Synchronous systems, the output of all the digital circuits changes

When an enable signal is applied instead of the clock signal.

Select correct option:

- True
- False Page228

_____ flip-flops are obsolete now.

Learning With A&I

Select correct option:

- Edge-triggered
- Master-Slave Page257
- T-Flipflop
- D-Flipflop

A mono-stable device only has a single stable state----------

Select correct option:

- True Page262
- False

A transparent mode means _____

Select correct option:

- The changes in the data at the inputs of the latch are seen at the output (Page 245)
- The changes in the data at the inputs of the latch are not seen at the output
- Propagation Delay is zero (Output is immediately changed when clock signal is applied)
- Input Hold time is zero (no need to maintain input after clock transition)

If the S and R inputs of the gated S-R latch are connected together using a _____ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

Select correct option:

- AND
- OR

Learning With A&I

- NOT Page226
- XOR

When an eight bit serial in/serial out shift register is used for a 24 micro seconds time delay, the clock frequenct must be Select correct option:

Select correct option:

- 41.67 KHz
- 333 KHz
- 125 KHz
- 8 MHz

A modulus-14 counter has fourteen states requiring_____

Select correct option:

- 14 Flip Flops
- 14 Registers
- 4 Flip Flops
- 4 Registers

RCO Stands for _____

Select correct option:

- Reconfiguration Counter Output
- Reconfiguration Clock Output
- Ripple Counter Output
- Ripple Clock Output (Page 285)

Karnaugh map is used in designing Select correct option:

Learning With A&I

Select correct option:

- A clock
- A counter
- An UP/DOWN counter
- All of the above

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=

Select correct option:

- 1
- 0

The power consumed by a flip-flop is defined by _

Select correct option:

- P = Vcc x Icc Page235
- P = Icc x Rcc
- P = Vcc x Rcc
- P = Mcc x Vcc

The terminal count of a 4-bit binary counter in the DOWN mode is

Select correct option:

- 0000
- 0011
- 1100
- 0010

Memories are implemented in bit data unit sizes

Learning With A&I

Select correct option:

- 1 , 2 and 6
- 2 , 3 and 6
- 1 , 4 and 8 page 425
- 4 , 5 and 8

Flip flops are also called_____.

Select correct option:

- Bi-stable multivibrators Page228
- Bi-stable singlevibrators
- Bi-stable dualvibrators
- Bi-stable transformer

The low to high or high to low transition of the clock is considered to be a(n) _____

Select correct option:

- Edge Page228
- Add
- Odd
- Out

Subtractors also have output to check if 1 has been _____.

Select correct option:

- Primed
- Shifted
- Complemented

Learning With A&I

- Borrowed

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minter) present in the expression.

Select correct option:

- 1 Page90
- 2
- 3
- 4

Two Signals and provide the timing inputs to the state machine

Select correct option:

- NSSR and EWSR
- LTIME and STIME page 374
- PTIME and QTIME
- NSGrn and NSYel

Two signals _____ and _____ provide the timing inputs to theState Machine.

Select correct option:

- LTIME and STIME Page374
- NSSR and EWSR
- LTIME and STIME
- PTIME and QTIM

Learning With A&I

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

Select correct option:

- -WE Page397
- CS
- OE

The output of a NAND gate is _____ when all the inputs are one.

Select correct option:

- Zero Page47
- One
- Available
- Not available

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minters) with an 8-input OR gate.

Select correct option:

- 8 AND
- 8 And
- 8 OR
- None of these

If the FIFO Memory output is already filled with data then _____

Learning With A&I

Select correct option:

- It is locked; no data is allowed to enter
- It is not locked; the new data overwrites the previous data.
- Previous data is swapped out of memory and new data enters
- None of given options

3-to-8 decoder can be used to implement Standard SOP and POS boolean expressions

Select correct option:

- True Page161
- False

If a circuit suffers "Clock Skew" problem, the output of circuit can't be guaranteed.

Select correct option:

- True
- False

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

Select correct option:

- Nand
- NOT
- OR
- AND

Learning With A&I

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

Select correct option:

- High Page417
- Low
- Medium
- Hot

The total amount of memory that is supported by any digital system depends upon _____

Select correct option:

- The organization of memory
- The structure of memory
- The size of decoding unit
- The size of the address bus of the microprocessor (Page 430)

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

Select correct option:

- True
- False

A multiplexer with a register circuit converts

Learning With A&I

Select correct option:

- Parallel data to serial Page356
- Serial data to parallel
- Serial data to serial
- Parallel data to parallel

Implementation of Latch is required almost _____ transistor.

Select correct option:

- Six Page417
- Two
- Three
- Four

The Synchronous SRAM also has a Burst feature which allows the synchronous SRAM to read or write up to _____ location(s) using a single address.

Select correct option:

- One
- Two
- Three
- Four Page399

LUT is acronym for _____

Select correct option:

- Look Up Table (Page 439)
- Local User Terminal
- Least Upper Time Period
- None of given options

Learning With A&I

Consider A=1, B=0, C=1. A, B and C represent the input of three-bit NAND gate, the output of the NAND gate will be _____.

Select correct option:

- One Page46
- Two
- Three
- Four

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

Select correct option:

- 1
- 2
- 3
- 4 Page278

The _____ input overrides the _____ input.

Select correct option:

- Asynchronous, synchronous Page369
- Synchronous, asynchronous
- Preset input (PRE), Clear input (CLR)
- Clear input (CLR), Preset input (PRE)

The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

Select correct option:

- Three Page362
- Four
- Five
- Two

Learning With A&I

A decade counter is _____.

Select correct option:

- Mod-3 counter
- Mod-5 counter
- Mod-8 counter
- Mod-10 counter (Page 274)

The counter states or the range of the number of a counter is determined by the formula("n" represented the total number of flip-flops)

Select correct option:

- 2 raise to power n
- (n raise to power 2)
- (n raise to power 2 and then minus 1)
- (2 raise to power n and then minus 1)

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in number of states in an 8-bit Johnson counter sequence are:

Select correct option:

- 16
- 8
- 32
- 64

Learning With A&I

UVEPROM is stands for----------

Select correct option:

- Ultra-Violet Erasable Programmable Read Only Memory.
- Ultra-Violet Erasable Programmable Random Only Memory.
- Ultra-Violet Erasable Program Read Only Memory.
- None of these

The synchronous counters are also known as Ripple Counters:

Select correct option:

- False
- True

The _____ input overrides the _____ input

Select correct option:

- Asynchronous, synchronous (Page 369)
- Synchronous, asynchronous
- Preset input (PRE), Clear input (CLR)
- Clear input (CLR), Preset input (PRE)

A memory organized to store nibble data values requires a _____ wide data bus.

Select correct option:

- 4-bit Page390
- 8-bit
- 16-bit
- 32-bit

Learning With A&I

The chip enable access time which is the time for the valid data to appear after the _____ transition of the chip select signal ¯CS.

Select correct option:

- High-to-low Page397
- Low -to-High
- Both A&B
- None of these

In asynchronous digital systems all the circuits change their state with respect to a common clock

Select correct option:

- False Page245
- True

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____

Select correct option:

- Set-up time Page234
- Hold time
- Pulse Interval time
- Pulse Stability time (PST)

Learning With A&I

74HC163 has two enable input pins which are _____ and _____

Select correct option:

- ENP, ENT (Page 285)
- ENI, ENC
- ENP, ENC
- ENT, ENI

Which of the following is a volatile memory?

Select correct option:

- DRAM
- PROM
- EPROM
- EEPROM

The combinational digital circuits have _____ storage element; therefore combinational circuits handle only instantaneous inputs.

Select correct option:

- No Page210
- Yes

In the keyboard encoder, how many times per second does the ring counter scan the key board?

Select correct option:

- 650 scans/second
- 600 scans/second
- 625 scans/second
- 700 scans/second

Learning With A&I

The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.

Select correct option:

- 1
- 2
- 3
- 4

_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Select correct option:

- Combinational Input/Output Page185
- Combinational Input/Output
- Combinational Output
- Programmable polarity

A frequency counter _

Select correct option:

- Counts pulse width
- Counts no. of clock pulses in 1 second (Page 301)
- Counts high and low range of given clock pulse
- None of given options

Learning With A&I

A 3-variable Karnaugh map has

Select correct option:

- Eight cells Page89
- Three cells
- Sixteen cells
- Four cells

The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

Select correct option:

- Truth Table Page370
- State Diagram
- Karnaugh Map
- Logic Circuit

In DRAM read cycle R /W- signal is activated to read data which is made available **on the _____ data line.**

Select correct option:

- D(IN)
- D(OUT) Page405
- D(AB)
- D(INT)

Learning With A&I

In _____, all the columns in the same row are either read or written.

Select correct option:

- Sequential Access
- MOS Access
- FAST Mode Page Access (Page 413)
- None of given options

A SOP expression can be implemented by an _____ combination of

Select correct option:

Gates.

- AND-OR Page78
- OR-XOR
- AND-NAND
- XOR-NOR

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

Select correct option:

- 8 Page356
- 4
- 16
- 32

Learning With A&I

The terminal count of a modulus -13 binary counter is

Select correct option:

- 1101
- 1100
- 1011
- 1110

A multiplexer with a register circuit converts _____

Select correct option:

- Serial data to parallel
- Parallel data to serial (Page 356)
- Serial data to serial
- Parallel data to parallel

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

Select correct option:

- Column, row Page191
- Column, row
- Column, column
- Row, row

The Transition table is very similar to the _____ table.

Select correct option:

- State Page382
- Truth
- State
- Transition

Learning With A&I

Two types of memories namely the first in-first out (FIFO) memory and Last in first out (LIFO) are implemented using _____.

Select correct option:

- Shift Registers Page417
- Circular Buffers
- Ring Buffers
- Reduce Registers

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

Select correct option:

- Doesn't have an invalid state (Page 232)
- Sets to clear when both J = 0 and K = 0
- It does not show transition on change in pulse
- It does not accept asynchronous inputs

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

Select correct option:

- 110
- 101
- 100
- 001

Learning With A&I

The terminal count of a 4-bit binary counter in the UP mode is _____.

Select correct option:

- 1111
- 1011
- 1110
- 0010

Select the mode of programming in which GAL16V8 can be programmed:

Select correct option:

- Simple Mode
- Complex Mode
- Registered Mode
- All of the given

In a state diagram, the transition from a current state to the next state is determined by

Select correct option:

- Current state and the inputs (Page 332)
- Current state and outputs
- Previous state and inputs
- Previous state and outputs

Learning With A&I

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

Select correct option:

- 256
- 257
- 258
- 259

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

Select correct option:

- 1001
- 1000
- 1100
- 1011

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

Select correct option:

- NAND, NAND Page211
- NOR, NAND
- NAND, NOR
- NOR, NOR

Learning With A&I

The address from which the data is read, is provided by _____

Select correct option:

- Depends on circuitry
- RAM
- Microprocessor (Page 397)
- None of given options

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

Select correct option:

- REQ0
- OPEN
- REQ1 Page370
- FLOOR1

A decade counter is _____

Select correct option:

- Mod-3 counter
- Mod-5 counter
- Mod-8 counter
- Mod-10 counter Page274

Learning With A&I

PALs tend to execute _____ logic.

Select correct option:

- SPD
- SOP
- SAC
- SAP

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

Select correct option:

- 2
- 4
- 8 Page272
- 10

A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is----------

Select correct option:

- 0001
- 1000
- 1110
- 1111

Learning With A&I

An Astablemultivibrator is known as a(n) _____

Select correct option:

- Oscillator Page258
- Booster
- One-shot
- Dual-shot

Flash memory Operation are classified into _____ different operation.

Select correct option:

- One
- Two
- Three Page413
- Four

5-bit Johnson counter sequences through ____ states

Select correct option:

- 7
- 10 (Page 354)
- 32
- 25

In designing any counter, the transition from a current state to the next sate is determined by-------

Select correct option:

- Current state and inputs Page332
- Only inputs Only current state
- Positive-Edge triggered
- Negative-Edge triggered

Learning With A&I

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Select correct option:

- Race condition
- Clock Skew Page226
- Ripple Effect
- None of given options

A latch is a temporary storage device that has _____ stable states.

Select correct option:

- Two Page211
- Three
- Four
- Five

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

Select correct option:

- XOR, NAND
- NOR, XOR
- NOR, NAND Page213
- OR, XOR

Learning With A&I

RCO stands for _____

Select correct option:

- Reconfiguration Counter Output
- Ripple Counter Output
- Reconfiguration Clock Output
- Ripple Clock Output Page285

According to Moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.

Select correct option:

- Previous state
- Present state
- Next state
- External state

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

Select correct option:

- NOT
- AND Page372
- OR
- XOR

Learning With A&I

In memory write cycle, the time for which the WE signal remains active is known as the _____.

Select correct option:

- Write address setup
- Write pulse width Page397
- Write delay width
- Write data time

_____ is one of the examples of synchronous inputs.

Select correct option:

- J-K input Page235
- EN input
- Preset input (PRE)
- Clear Input (CL

There are _____ possible combinations of the Simple Mode in which OLMC can be configured.

Select correct option:

- Three Page201
- Four
- Five
- Six

Learning With A&I

Once the state diagram is drawn for any sequential circuit the next step is to draw

Select correct option:

- Transition table
- Karnaugh map
- Next- state table
- Logic expression

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

Select correct option:

- 0
- 1
- 2
- 3

If S=1 and R=0, then for positive edge triggered flip-flop

Select correct option:

- 0
- 1 Page230
- 2
- 3

A negative edge-triggered flip-flop changes its state when---------

Select correct option:

- Enable input (EN) is set
- Preset input (PRE) is set
- Low-to-high transition of clock
- High-to-low transition of clock (Page 228)

Learning With A&I

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

Select correct option:

- Two
- Four Page212
- Eight
- Sixteen

Three cascaded modulus-10 counters have an overall modulus of Select Correct option

- 30
- 100
- 1000
- 10000

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

Select correct option:

- 4.8 microsec
- 5.9 microsec
- 7.8 microsec Page406
- 5.5 microsec

Learning With A&I

A Divide-by-20 counter can be achieved by using

Select correct option:

- Flip-Flop and DIV 10
- Flip-Flop and DIV 16
- Flip-Flop and DIV 32
- Div 10 and DIV 16

The terminal count of a modulus-13 binary counter is Select correct option:

- 0000
- 1111
- 1101
- 1100

A synchronous decade counter will have _____ flipflops.

Select correct option:

- 3
- 4 Page281
- 7
- 10

Divide-by-32 counter can be achieved by using----------

Select correct option:

- Flip-Flop and DIV 10
- Flip-Flop and DIV 16
- Flip-Flop and DIV 32
- DIV 16 and DIV 32

Learning With A&I

The 64-cell array organized as 8 x 8 cell array is considered as an 64

Select correct option:

- Byte memory
- As a 16 byte memory
- As an 8 byte memory Page387
- As an 4 byte memory

_____ Counters as the name indicates are not triggered simultaneously

Select correct option:

- Asynchronous Page262
- Synchronous
- Positive-Edge triggered
- Negative-Edge triggered

You have to choose suitable option when your timer will reset by

Considering this given code:

TRSTATE.CLK = clk;

TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

Select correct option:

- NSY2 or EWY2
- NSSR or TMRST
- EWSR or NSRED
- EWRed or EWYel

Learning With A&I

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

Select correct option:

- True
- False

_____ is used to minimize the possible no. of states of a circuit.

Select correct option:

- State assignment (Page 341)
- State reduction
- Next state table
- State diagram

_____ is one of the examples of asynchronous inputs.

Select correct option:

- J-K input
- S-R input
- D input
- Clear Input (CLR) (Page 235)

Learning With A&I

Cs302 Final Term Most Important MCQs

آپ سب سے گزارش ہے پلیز دعاؤں میں یاد رکھیں

مزید ایسی پوسٹ حاصل کرنے کیلئے ہمارا یوٹیوب چینل سبسکرائب کریں

اللہ پاک آپ سب کو اور مجھے اپنے مشن میں کامیابی عطا فرمائے۔۔۔آمین

- Short Notes
- Important Question
- Repeated Question
- Final term
- Mid term
- Current Paper
- Moaz Past Solved Paper

- Waqar Siddu Past Solved Paper
- Solved Paper
- Past Paper
- Quiz File
- Assignment
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