

CS302- Digital Logic and Design

QUIZ-2

Solved by JUNAID MALIK



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- 1) SRS
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- 2) DD
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- 4) Viva preparation
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ALL answers are verified if found any mistake then Correct ACCORDINGLY

1. The transition table is very similar to the _____ table
 - a. Truth
 - b. **State** page 382
 - c. Transition
 - d. None of the given option
2. Two Signals _____ and _____ provide the timing inputs to the state machine
 - a. NSSR and EWSR
 - b. **LTIME and STIME** page 374
 - c. PTIME and QTIME
 - d. NSGrn and NSYel
3. Memories are implemented in _____ bit data unit sizes
 - a. 1, 2 and 6
 - b. 2, 3 and 6
 - c. **1, 4 and 8** page 425
 - d. 4, 5 and 8
4. In distributed mode, for a 1024 X 1024 DRAM memory and a refresh cycle of 8msec, each of the 1024 rows has to be refreshed in _____ when distributed refresh is used
 - a. 4.8 microsec
 - b. 5.9 micorsec
 - c. **7.8 micorsec** page 406
 - d. 5.5 microsec
5. The EPROM uses _____ array with an isolated gate structure
 - a. **NMOSFET** page 411
 - b. MOSFETK
 - c. UVMOSFT
 - d. None of the given options
6. The 64-cell array organized as 8 X 8 cell array is considered
 - a. As an 64 byte memory
 - b. As a 16 byte memory
 - c. **As an 8 byte memory** page 387
 - d. As an 4 byte memory
7. The test vector definition defines the test vector for all the three counter inputs and _____ counter output/outputs

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- a. One
 - b. Two
 - c. **Three** page 362
 - d. Four
8. In memory write cycle, the time for which the WE signal remains active is known as the _____
- a. Write address setup
 - b. **Write pulse width** page 397
 - c. Write delay width
 - d. Write Data Time
9. If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____
- a. 0
 - b. **1** page 417
10. As data values are written or read from RAM stack, the stack pointer register increments or decrements its contents always pointing to the stack _____
- a. Bottom
 - b. **Top** page 422
 - c. Down
 - d. Vertex
11. A 4-bit binary up/down counter in the binary state of zero. The next state in the DOWN mode is?
- a. 0001
 - b. 1000
 - c. 1110
 - d. **1111**
12. Flash memory operation are classified into _____ different operations
- a. Two
 - b. **Three** page 413
 - c. Four
 - d. Five
13. Implementation of latch is required almost _____ transistor?
- a. Two
 - b. Four
 - c. **Six** page 417
 - d. Eight
14. In elevator circuit, the floor display circuit is a combinational circuit which uses the _____ and _____ inputs to determine the floor number and the function of the display arrow.

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- a. CONSTATE, FB
 - b. OPEN, DIR
 - c. **MOTION, DIR** page 374
 - d. MOTION, FB
15. The bit capacity of memory that has 1024 addresses and can store 8 bit at each address is
- a. 8
 - b. 1024
 - c. 4096
 - d. **8192** page 388 (memory capacity) $1024 \times 8 = 8192$
16. When the transmission line is idle in an asynchronous transmission
- a. It is set to logic low
 - b. **It set to logic high** page 349
 - c. It remains in previous state
 - d. State of transmission line is not used to start transmission
17. Which of the following is a volatile memory?
- a. PROM
 - b. **DRAM** page 400 (capacitor based ROM, need extra circuit to retain the memory)
 - c. EPROM
 - d. EEPROM
18. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration t_{WD} ?
- a. $\overline{CS}$
 - b. **$\overline{WE}$** page 397
 - c. W
 - d. OE
19. The ROM used by computer is relatively very _____ as it stores few bytes of code used to boot the computer system on power up
- a. **Small** page 423
 - b. Large
 - c. Heavy
 - d. High
20. In DRAM read cycle R/W signal is activated to read data which is made available on the Data line
- a. D(IN)
 - b. **D(OUT)** page 405
 - c. D(AB)

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- d. D(INT)
21. _____ Yellow signal controlling the traffic on the east–west section.
- a. NSGrn
 - b. NSYel
 - c. EWYel page 375
 - d. EWRed
22. A 32 bit data word consists of :
- a. 2 bytes
 - b. 4 Bytes page 387
 - c. 2 nibbles
 - d. 4 nibbles
23. A complete unit of information is sometimes called a _____
- a. Bit
 - b. Nibble
 - c. Word(correct) page 387
 - d. Byte
24. Memory is arranged in
- a. Linear fashion
 - b. Two dimensional manner page 396
 - c. Three dimensional manner
 - d. Random fashion
25. Which of the following output equations determines the output of the state machine?
- a. $MIN = Q0Q1$
 - b. $MAX = Q0Q1EN$ page 382
 - c. $MIN = Q0Q1EN$
 - d. $MAX = Q1EN$
26. A multiplexer with the register circuit convert
- a. Serial data to parallel
 - b. Parallel data to serial page 349
 - c. Serial data to serial
 - d. Parallel data to parallel
27. The chip enable access time which is the timer for the validated data to appear after the transition of the chip select signal CS
- a. high to high
 - b. high to low page 397
 - c. low to high

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- d. low to low
28. The duration for which the elevator doors are opened , and remain open,, and time it takes for elevator to move from one floor to the next can be determined by a/an___
- a. input signal
 - b. output signal
 - c. clock signal page 365
 - d. None of Given
29. The ABEL input file can use a _____ instead of the equation to specify the Boolean expression
- a. truth table page 370
 - b. state diagram
 - c. karnaugh map
 - d. logical circuit
30. Implementation of the FIFO buffer in RAM is usually takes the form of a _____ buffer
- a. Circular page 420
 - b. Rectangular
 - c. Triangular
 - d. Square
31. How many state variables does each state in Traffic Light Controller have?
- a. One
 - b. Two
 - c. Three page 377
 - d. Four
32. The output of SR latches in elevator state machine are generated by combinational circuit therefore these output are defined as ISTYPE _____
- a. Com.reg
 - b. Com.org
 - c. Com.buffer page 372
 - d. Reg.buffer
33. When an eight bit serial in/out shift register is used for 24 micro second time delay the clock frequency must be
- a. 41.67 KHz
 - b. 333 KHz
 - c. 125 KHz
 - d. 8 MHz

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34. Which of the following memories uses one transistor and one capacitor as basic memory unit?

- a. SRAM
- b. DRAM page 400
- c. PRAM
- d. TRAM

35. A divide by 10 ring counter requires a minimum of a. Ten flip flops

- b. Five flip flops
- c. Four flip flops
- d. Twelve flip flops

35. Which one flip flop has an invalid output state?

- a. T
- b. J
- c. K
- d. SR

36. In the keyboard encounter how many times per second does the ring counter scan the keyboard

- a. 600 scans./second
- b. 625 scan/second
- c. 650 scan/second
- d. 700 scan/second

37. Smallest unit of data

- a. a bit
- b. a 4 bit nibbles
- c. an 8 bit word
- d. a 16 bit word

38. The output of SR latches in elevator state machine are feed back to the _____ gate array for connection of D Flip Flops

- a. NO
- b. T
- c. AND
- d. OR
- e. XOR

39. The static RAM(SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information

- a. Low
- b. High

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- c. Medium
 - d. Hot
40. Choose the best possible answer of the following question.
The D flip flop is only activated by _____
- a. A negative edged trigger
 - b. A positive edged trigger
 - c. Both positive and negative edge triggered
 - d. None of the given options
41. The Fast mode page access allows _____ memory read and access time when reading successive data values stored in connective locations on the samerow
- a. Slo
 - w b. Faster
 - c. Medium
 - d. Modern
42. The next state table for REQ1, FLOOR1 and OPEN input indicates that the _____ can be pressed at any time either on the first floor or the second floor inelevator
- a. REQ0
 - b. Open
 - c. REQ I
 - d. FLOOR1
49. A 4-bit binary up/down counter in in the binary state of zero. The next state in the UP mode is?
- 0001
 - 1000
 - 1110
 - 1111
50. In memory read cycle, the read cycle is initiated by
- a. Providing data to the variable
 - b. Applying data to signals
 - c. Applying the address signals
 - d. Providing arithmetic operations
51. FLASH memory cell is implemented using a single floating gate _____ transistor
- a. MOS
 - b. LOS

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- c. GOS
- d. POS

52. UVEPROM stands for

- a. Ultra Variant
- b. Ultra Vibrant
- c. Ultra Violet
- d. Ultra Visible

53. Four 4k byte chips can be connected together to implement word memory

- a. 10K
- b. 15K
- c. 16K
- d. 8K

54. There are _____ basic type of EPROM

- a. Two
- b. Three
- c. Four
- d. Five

55. Two types of memories namely the first in first out (FIFO) memory and last in first out (LIFO) are implemented using _____

- a. Shift Register
- b. Circular Buffer
- c. Ring Buffer
- d. Reduce Registers

56. A memory organized to store nibble data values requires a _____ wide databus

- 2 bit
- 4 bit
- 8 bit
- 16 bit

57. ROMs and PROMs retain information _____ even if the supply voltage is removed.

- a. For one day
- b. For seven days
- c. For ten

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days

d.

Permanently

58. You have to choose suitable option when your timer will reset by considering this given code:

TRSTATE.CLK = clk;

TMRST: = (TRSTATE == NSY2) # (TRSTATE == EY2);

a. NSY2 or EY2

b. NSSR or TMRST

c. EWSR or NSRED

d. EWRed or EYel

59. Synchronous SRAM uses a clock signal which is used by the to synchronize its activities.

a. ALU

b. Control Unit

c. Microprocessor

d. Address Bus

60. Implementation of the FIFO buffer in _____ is usually takes the form of acircular buffer

a. RAM page 420

b. ROM

c. PROM

d. Flash Memory

61. The CONSTATE.CLK = Clock is used to indicate that the state variables change on a clock transition.

a. CONSTATE

b. FLOOR

c. MOTION

d. OPEN

62. The normal data inputs to a flip flop (D,S and R,J and K,T are referred) to as _____ inputs

a. Sequential

b. Asynchronous

us

c. Synchronous

d. Combinational

63. The synchronous SRAM also has a burst feature which allows the

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synchronous SRAM to read or write upto location(s) using a single address

- a. One
 - b. Two
 - c. Three
 - d. Four page 399
64. Two State variable allow maximum of _____ states
- a. Two
 - b. Four page 381
 - c. Eight
 - d. Sixteen
65. Which of the following is the drawback of DRAM?
- a. Discharging of the capacitor over a period of time
 - b. All the information stored in terms of binary bits would be lost if capacitor is not recharged
 - c. Extra circuit is required to reference the capacitor
 - d. All of the above are true page 400
66. To write data to the memory the write cycle is initiated by
- a. Applying the address signals 397
 - b. Assigning the values of variable
 - c. Reserving the space of variables
 - d. Applying the data signals