

RIZ MUGHAL

QUIZ MASTER

CS302 QUIZ 1 (Lec 23 to 32)

100% correct solution.

For more information you can visit my channel and for any type of help related to CS619 you can contact me.



YOUTUBE CHANNEL:

<https://www.youtube.com/channel/UCINsFwDiB62SValCcPDZbRQ/playlists>

FACEBOOK GROUP:

<https://www.facebook.com/groups/923887914750307>

CS302:Semester Quiz # 01

Question # 1 of 10 (Start time: 12:07:20 AM, 28 Ja

A decade counter is _____

Select the correct option

- | | |
|----------------------------------|----------------|
| ☐ | Mod-3 counter |
| ☐ | Mod-5 counter |
| ☐ | Mod-8 counter |
| ☒ | Mod-10 counter |

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Question # 2 of 10 (Start time: 12:07:35 AM, 28 January 2021)

If $S=1$ and $R=0$, then for positive edge triggered flip-flop
 $Q(t+1) =$ _____

Select the correct option

☐	0
☒	1
☐	Invalid
☐	Input is invalid

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Question # 3 of 10 (Start time: 12:07:55 AM, 28 January 2021)

A positive edge-triggered flip-flop changes its state when _____

Select the correct option

- | | |
|----------------------------------|---------------------------------|
| ☐ | Enable input (EN) is set |
| ☐ | Preset input (PRE) is set |
| ☒ | Low-to-high transition of clock |
| ☐ | High-to-low transition of clock |

Question # 4 of 10 (Start time: 12:08:08 AM, 28 January 2021)

Total Marks:

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

Select the correct option

☒	True	//
☐	False	//

Question # 5 of 10 (Start time: 12:08:23 AM, 28 January 2021)

Total Ma

When the ____ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of ____ seconds.

Select the correct option



1,2



0,2



2,5



1,1

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Question # 6 of 10 (Start time: 12:08:41 AM, 28 January 2021)

The n flip-flops store _____ states.

Select the correct option

☐	1
☒	2^n
☐	0
☐	$2^{(n+1)}$

Question # 7 of 10 (Start time: 12:08:54 AM, 28 January 2021)

T

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____

Select the correct option

☒	Set-up time
☐	Hold time
☐	Pulse Interval time
☐	Pulse Stability time (PST)

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Question # 8 of 10 (**Start time: 12:09:11 AM, 28 January 2021**)

A Divide-by-20 counter can be achieved by using

Select the correct option

☒	Flip-Flop and DIV 10
☐	Flip-Flop and DIV 16
☐	Flip-Flop and DIV 32
☐	Div 10 and DIV 16

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Question # 9 of 10 (Start time: 12:09:26 AM, 28 January 202

The Synchronous counters are also known as Ripple Counters:

Select the correct option



True



False

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Question # 10 of 10 (Start time: 12:09:55 AM, 28 January 2021)

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is _____

Select the correct option

- | | |
|----------------------------------|------|
| ☐ | 0001 |
| ☒ | 1111 |
| ☐ | 1000 |
| ☐ | 1110 |

2nd account

Question # 1 of 10 (Start time: 12:19:40 AM, 28 January 2021)

_____ is said to occur when multiple internal variables change due to change in one input variable

Select the correct option

- | | |
|----------------------------------|----------------|
| ☐ | Hold and Wait |
| ☐ | Clock Skew |
| ☒ | Race condition |
| ☐ | Hold delay |

Question # 2 of 10 (Start time: 12:19:58 AM, 28 January 2021)

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is _____

Select the correct option

☐	0001
☒	1111
☐	1000
☐	1110

Question # 3 of 10 (Start time: 12:20:17 AM, 28 January 2021)

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and K be?

Select the correct option

- | | |
|----------------------------------|--------------------------|
| ☐ | J = 1, K = 0 |
| ☐ | J = 1, K = X(Don't care) |
| ☒ | J = X(Don't care), K = 0 |
| ☐ | J = 0, K = X(Don't care) |

Question # 4 of 10 (Start time: 12:20:42 AM, 28 January 2021)

In Master-Slave flip-flop the Clock signal is connected to Slave flip-flop using _____ gate

Select the correct option

☐	AND
☐	OR
☒	NOT
☐	NAND

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Question # 5 of 10 (Start time: 12:20:58 AM, 28 January 2021)

Each stage of Master-slave flip-flop works at ____ of the clock signal

Select the correct option

☐	Each stage works on complete clock signal
☐	One fourth
☐	One third
☒	One half

Question # 6 of 10 (Start time: 12:21:14 AM, 28 January 2021)

Total Marks:

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

Select the correct option

☒	True	//
☐	False	//

Question # 7 of 10 (Start time: 12:21:38 AM, 28 January 2021)

Total Marks:

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using

Select the correct option

- | | | |
|----------------------------------|---------------------|----|
| ☐ | Using S-R Flop-Flop | // |
| ☐ | D-flipflop | // |
| ☒ | J-K flip-flop | // |
| ☐ | T-Flip-Flop | // |

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Question # 8 of 10 (Start time: 12:21:55 AM, 28 January 2021

A Divide-by-20 counter can be acheived by using

Select the correct option

- | | |
|----------------------------------|----------------------|
| ☒ | Flip-Flop and DIV 10 |
| ☐ | Flip-Flop and DIV 16 |
| ☐ | Flip-Flop and DIV 32 |
| ☐ | Div 10 and DIV 16 |

Question # 9 of 10 (Start time: 12:22:09 AM, 28 January 2021)

Total Marks: 1

If the S and R inputs of the gated S-R latch are connected together using a _____ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

Select the correct option

☐	AND	//
☐	OR	//
☒	NOT	//
☐	XOR	//

[Click to Save Answer & Move to Next Question](#)

Question # 10 of 10 (Start time: 12:22:36 AM, 28 January 2021)

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

Select the correct option

☐	Set-up time
☒	Hold time
☐	Pulse Interval time
☐	Pulse Stability time (PST)

Thank you For Watching😊

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