

VIRTUAL UNIVERSITY OF PAKISTAN

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CORRECT ANSWER SOLVED BY HADI
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TEAM HADI(VU LAHORE)

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Best of luck!



Question No : 1 of 26

Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the FALCON-A processor?

Answer (Please select your correct option)

☐ 8 bits

☐ 16 bits

☐ 32 bits

☐ 64 bits

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Question No : 2 of 26

Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the SRC processor?

Answer (Please select your correct option)

☐ 8 bits

☐ 16 bits

☐ 32 bits

☐ 64 bits

✓
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Question No : 3 of 26

Marks: 1 (Budgeted Time 1 Min)

What does the word 'D' in the 'D-flip-Flop' stands for?

Answer (Please select your correct option)

☐ Double

☐ Data

☐ Digital

☐ Dynamic

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Question No : 4 of 26

Marks: 1 (Budgeted Time 1 Min)

"If $P = 1$, then load the contents of register R1 into register R2".
This statement can be written in RTL as:

Answer (Please select your correct option)

- ☐ $R1 \leftarrow R2$
- ☐ $P: R1 \leftarrow R2$
- ☐ $P: R2 \leftarrow R1$
- ☐ $P: R2 \leftarrow R1, P: R1 \leftarrow R2$

✓
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Question No : 5 of 26

Marks: 1 (Budgeted Time 1 Min)

Almost every commercial computer has its own particular ----- language

Answer (Please select your correct option)

☐ assembly language

☐ English language

☐ Higher level language

☐ 3GL

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Question No : 6 of 26

Marks: 1 (Budgeted Time 1 Min)

A ----- is a computer program that is used to test and debug other programs.

Answer (Please select your correct option)

☐ Linker

☐ Loader

☐ Debugger

☐ Compiler



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Question No : 7 of 26

Marks: 1 (Budgeted Time 1 Min)

What is the working of **Processor Status Word (PSW)**?

Answer (Please select your correct option)

- ☐ To hold the current status of the processor.
- ☐ To hold the address of the current process
- ☐ To hold the instruction that the computer is currently processing
- ☐ To hold the address of the next instruction in memory that is to be executed

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Question No : 8 of 26

Marks: 1 (Budgeted Time 1 Min)

The instruction -----will **load** the register R3 with the contents of the memory location M [PC+56]

Answer (Please select your correct option)

☐ Add R3, 56

☐ lar R3, 56

☐ ldr R3, 56

☐ str R3, 56

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Question No : 9 of 26

Marks: 1 (Budgeted Time 1 Min)

Motorola MC68000 is an example of -----microprocessor.

Answer (Please select your correct option)

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☐ CISC

☐ RISC

☐ SRC

☐ FALCON

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Question No : 10 of 26

Marks: 1 (Budgeted Time 1 Min)



_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

Answer (Please select your correct option)

☐ INC4

☐ LPC

☐ PCout

☐ LC

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Question No : 11 of 26

Marks: 1 (Budgeted Time 1 Min)

op<4.0>:= IR<15..11>:

The above RTL instruction presents the _____ of the FALCON-A Instructions.

Answer (Please select your correct option)

- ☐ operation code field
- ☐ target register field
- ☐ operand or address index
- ☐ second operand

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Question No : 12 of 26

Marks: 1 (Budgeted Time 1 Min)

_____ operation is required to change the processor's state to a known, defined value.

Answer (Please select your correct option)

☐ Change

☐ Reset

☐ Update

☐ Halt

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Question No : 13 of 26

Marks: 1 (Budgeted Time 1 Min)

_____ is/are defined as the number of instructions processed per second

Answer (Please select your correct option)

☐ Throughput

☐ Latency

☐ Hazards

☐ Throughput and Latency

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Question No : 14 of 26

Marks: 1 (Budgeted Time 1 Min)

Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

Answer (Please select your correct option)

- ☐ Instruction Register
- ☐ Memory address register
- ☐ Memory Buffer Register
- ☐ Registers A and C



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Question No : 15 of 26

Marks: 1 (Budgeted Time 1 Min)

Anything that interrupts the normal flow of execution of instructions in the processor is called a/an -----

Answer (Please select your correct option)

☐ Function

☒ Exception

☐ Assembler

☐ Machine

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Question No : 16 of 26

Marks: 1 (Budgeted Time 1 Min)

In pipelining ----- is increased by overlapping the instruction execution

Answer (Please select your correct option)

- ☐ Latency
- ☒ Throughput
- ☐ Execution time
- ☐ Clock speed



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Question No : 17 of 26

Marks: 1 (Budgeted Time 1 Min)

_____ control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.

Answer (Please select your correct option)

☐ LPC



☐ INC4

☐ LC

☐ Cout

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Question No : 18 of 26

Marks: 1 (Budgeted Time 1 Min)

In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

Answer (Please select your correct option)

- ☒ Direct Addressing Mode
- ☐ Immediate addressing mode
- ☐ Indirect Addressing Mode
- ☐ Register (Direct) Addressing Mode



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Question No : 19 of 26

Marks: 1 (Budgeted Time 1 Min)

Which of the following hazard occurs when attempting to access the same resource in different ways at the same time?

Answer (Please select your correct option)

☐ RAW (read after write) data hazard

☒ Structural hazard

☐ Branch hazard

☐ Complex hazard



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Question No : 20 of 26

Marks: 1 (Budgeted Time 1 Min)

----- is the arithmetic portion of the Von Neumann architecture. It consists of registers, internal buses, arithmetic units and shifters.

Answer (Please select your correct option)

☐ Virtual Memory

☒ Data path

☐ Structural RTL

☐ Timing

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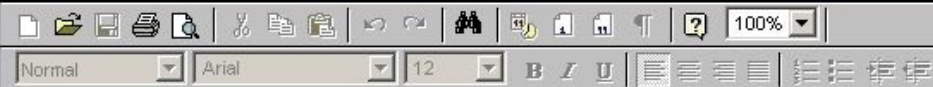
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Question No : 21 of 26

Marks: 2 (Budgeted Time 4 Min)

Compare the uni-bus implementation of FALCON-A with that of SRC with respect to size (Number of bits) of each register

Answer ([Please click here to Add Answer](#))



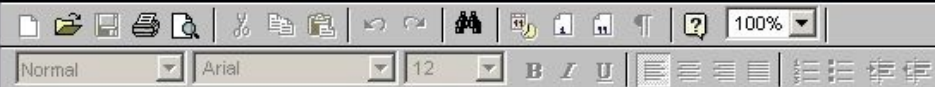
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Question No : 22 of 26

Marks: 2 (Budgeted Time 4 Min)

Differentiate between hard reset and soft reset?

Answer ([Please click here to Add Answer](#))



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Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

Write at least one advantage and one disadvantage of microprogramming.

Answer ([Please click here to Add Answer](#))



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Question No : 24 of 26

Marks: 3 (Budgeted Time 6 Min)

Write the Structural RTL for the “out” instruction i.e. **out ra, c2**.

Answer ([Please click here to Add Answer](#))



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Question No : 25 of 26

Marks: 5 (Budgeted Time 10 Min)

Write the related timing steps requirements and data path implementations of Instruction Fetch procedure using structural RTL

Answer ([Please click here to Add Answer](#))



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Question No : 26 of 26

Marks: 5 (Budgeted Time 10 Min)

What are three main problems related to pipelining? Describe any two of them.

Answer ([Please click here to Add Answer](#))

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