Digital Logic Design (CS302)
Multiple Choice Questions (MCQs)
Objective Questions

1. **In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.**
    1. True
    2. False
2. **Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.**
    1. Shift Registers
    2. Circular Buffers
    3. Ring Buffers
    4. Reduce Registers
    5. `
3. **The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.**
    1. One
    2. Two
    3. Three
    4. Four
4. **When the transmission line is idle in an asynchronous transmission**
    1. It is set to logic low
    2. It is set to logic high
    3. It remains in previous state
    4. State of transmission line is not used to start transmission
5. **A multiplexer with a register circuit converts**
    1. Serial data to parallel
    2. Parallel data to serial
    3. Serial data to serial
    4. Parallel data to parallel
6. **_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.**
    1. Combinational Input/Output
    2. Combinational Output
    3. Combinational Input
    4. Programmable polarity
7. **The terminal count of a 4-bit binary counter in the UP mode is _____.**

1. 1100
2. 0011
3. 1111
4. 0000

8. **A SOP expression can be implemented by an _____ combination of gates.**
   1. OR-XOR
   2. AND-NAND
   3. AND-OR
   4. XOR-NOR
9. **The n flip-flops store _____ states.**
   1. 1
   2. 2^n
   3. 0
   4. 2^(n+1)
10. **The AND Gate performs a logical _____ function.**
    1. Addition
    2. Substraction
    3. Multiplication
    4. Division
11. **The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.**
    1. two
    2. four
    3. eight
    4. sixteen
12. **Implementation of Latch is required almost _____ transistor.**
    1. Two
    2. Four
    3. Six
    4. Eight
13. **For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.**
    1. 0
    2. 1
    3. x (don't care condition)
    4. Any of given option depending on SOP term

14. **Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.**
    1. Negative-OR, Negative-AND
    2. Negative-AND, Positive-OR
    3. Positive-OR, Negative-AND
    4. Positive-OR, Positive-AND
15. **The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.**
    1. Sequential
    2. Asynchronous
    3. Synchronous
    4. Combinational
16. **The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.**
    1. One
    2. Two
    3. Three
    4. Four
17. **Select the mode of programming in which GAL16V8 can be programmed:**
    1. Simple Mode
    2. Complex Mode
    3. Registered Mode
    4. All of the given
18. **If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.**
    1. 0
    2. 1
19. **The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.**
    1. Small
    2. Large
    3. Heavy
    4. High
20. **In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.**
    1. NOR, NAND
    2. NAND, NOR
    3. NOR, NOR
    4. NAND, NAND
21. **The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.**

1. NOT
2. AND
3. OR
4. XOR

22. The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

1. REQ0
2. OPEN
3. REQ1
4. FLOOR1

23. The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

1. CONSTATE
2. FLOOR
3. MOTION
4. OPEN

24. A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

1. XOR, NAND
2. NOR, XOR
3. NOR, NAND
4. OR, XOR

25. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

1. Q output of all flip-flops to clock input of next flip-flops
2. Q' output of all flip-flops to clock input of next flip-flops
3. Q output of all flip-flops to J input of next flip-flops
4. Q' output of all flip-flops to K input of next flip-flops

26. Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

1. 64
2. 128
3. 256
4. 512

27. The 64-cell array organized as 8 x 8 cell array is considered

1. as an 64 byte memory
2. as a 16 byte memory
3. as an 8 byte memory
4. as an 4 byte memory

28. **Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.**
    1. RAM
    2. ROM
    3. PPROM
    4. Flash Memory

29. **If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.**
    1. 1001
    2. 0110
    3. 1111
    4. 1100

30. **In memory write cycle, the time for which the WE signal remains active is known as the _____.**
    1. Write address setup
    2. Write pulse width
    3. Write delay width
    4. Write data time

31. **Memory is arranged in _____.**
    1. linear fashion
    2. two-dimensional manner
    3. three-dimensional manner
    4. random fashion

32. **Cin is part of _____ Adder.**
    1. Half
    2. Full
    3. Single
    4. Double

33. **The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.**
    1. Slow
    2. Faster
    3. Medium
    4. Modern

34. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

1. True
2. False

35. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

1. 4.8 microsec
2. 5.9 microsec
3. 7.8 microsec
4. 5.5 microsec

36. The output of a NAND gate is _____ when all the inputs are one.

1. Zero
2. One
3. Available
4. Not available

37. Which of the following Output Equations determines the output of the State Machine?

1. MIN = Q0Q1
2. MAX = Q0Q1EN
3. MIN = Q0Q1EN
4. MAX = Q1EN

38. In the keyboard encoder, how many times per second does the ring counter scan the key board?

1. 600 scans/second
2. 625 scans/second
3. 650 scans/second
4. 700 scans/second

39. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1. 0001
2. 1000
3. 1110
4. 1111

40. The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

1. 2
2. 4
3. 6
4. 8

41. Divide-by-32 counter can be achieved by using

1. Flip-Flop and DIV 10
2. Flip-Flop and DIV 16
3. Flip-Flop and DIV 32
4. DIV 16 and DIV 32

42. If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

1. Different
2. Same
3. Equal
4. Opposite

43. The Transition table is very similar to the _____ table.

1. Truth
2. State
3. Transition
4. None of the given

44. GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

1. column, row
2. row, column
3. column, column
4. row, row

45. UVERPROM is stands for

1. Ultra-Variant
2. Ultra-Vibrant
3. Ultra-Voilet
4. Ultra-Visible

46. 8-bit parallel data can be converted into serial data by using _____ multiplexer.

1. 4-to-2
2. 8-to-1
3. 4-to-4
4. 8-to-4

47. Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

1. 8 OR
2. 8 AND
3. 8 XOR
4. 8 NOR

48. Why demultiplexer is called a data distributor?

1. The input will be distributed to one of the outputs
2. The input will be selected for the output
3. The output will be distributed to one of the inputs
4. Single input to Single Output

49. A 3-variable karnaugh map has

1. eight cells
2. three cells
3. sixteen cells

4. four cells

50. Flash memory Operation are classified into _____ different operation.

1. Two
2. Three
3. Four
4. Five

51. The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

1. Low
2. High
3. Medium
4. Hot

52. You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

1. NSY2 or EWY2
2. NSSR or TMRST
3. EWSR or NSRED
4. EWRed or EWYel

53. Which of the following is a volatile memory?

1. PROM
2. DRAM
3. EPROM
4. EEPROM

54. The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

1. Truth Table
2. State Diagram
3. Karnaugh Map
4. Logic Circuit

55. The domain of the expression AB'CD + AB' + C'D + B is

1. A and D
2. B only
3. A, B, C and D
4. None of the given

56. The maximum value, represented by a single hexadecimal digit is _____.

1. "E"
2. "F"
3. "G"
4. "H"

57. PALs tend to execute _____ logic.

1. SPD
2. SOP
3. SAC
4. SAP

58. Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

1. Zero
2. One
3. Undefined
4. No output as input is invalid

59. PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

1. PLAs
2. PALs
3. PLDs
4. EPROM

60. _____ Counters as the name indicates are not triggered simultaneously.

1. Asynchronous
2. Synchronous
3. Positive-Edge triggered
4. Negative-Edge triggered

61. Adding two octal numbers "36" and "71" result in _____.

1. 213
2. 123
3. 127
4. 345

62. In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.

1. D(IN)
2. D(OUT)

3. D(AB)
4. D(INT)

63. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

1. Bottom
2. Top
3. Down
4. Vertex

64. For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

1. 111
2. 110
3. 010
4. None of the given

65. Which one flip-flop has an invalid output state?

1. T
2. JK
3. SR
4. D

66. Two signals _____ and _____ provide the timing inputs to the State Machine.

1. NSSR and EWSR
2. LTIME and STIME
3. PTIME and QTIME
4. NSGrn and NSYel

67. The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.

1. 2
2. 4
3. 1
4. 0

68. Canonical form is a unique way of representing _____.

1. SOP
2. Minterm
3. Boolean Expression
4. POS

69. Subtractors also have output to check if 1 has been _____.

1. Primed
2. Shifted
3. Complemented
4. Borrowed

70. The _____ input overrides the _____ input.

1. Asynchronous, synchronous
2. Synchronous, asynchronous
3. Preset input (PRE), Clear input (CLR)
4. Clear input (CLR), Preset input (PRE)

71. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

1. $\overline{CS}$
2. $\overline{WE}$
3. W
4. OE

72. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

1. AND
2. NAND
3. OR
4. NOT

update answer if requir

CS302 – GRAND QUIZ BY JUNAID

Sr No.	MCQS QUESTION	ANSWER
1.	The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.	Faster
2.	In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.	NAND, NAND
3.	Why demultiplexer is called a data distributor?	Single input to Single Output
4.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input
5.	The n flip-flops store _____ states.	2^n
6.	The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.	NAND
7.	The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.	1
8.	As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.	Top
9.	In memory write cycle, the time for which the WE signal remains active is known as the _____.	Write pulse width
10.	You have to choose suitable option when your timer will reset by considering this given code: TRSTATE.CLK = clk; TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);	NSY2 or EWY2
11.	Two signals _____ and _____ provide the timing inputs to the State Machine.	PTIME and QTIME
12.	PALs tend to execute _____ logic.	SOP
13.	Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?	¯WE
14.	Memory is arranged in _____.	two-dimensional manner
15.	The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.	High
16.	Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.	8 AND
17.	The maximum value, represented by a single hexadecimal digit is _____.	“F”

18.	The _____ input overrides the _____ input.	Asynchronous, synchronous
19	A SOP expression can be implemented by an _____ combination of gates.	AND-OR
20.	The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.	AND
21.	The Transition table is very similar to the _____ table.	State
22.	The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.	Truth Table
23.	A 3-variable karnaugh map has	eight cells
24.	If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.	Same
25.	Adding two octal numbers "36" and "71" result in _____.	127
26.	Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.	One
27.	Subtractors also have output to check if 1 has been _____.	Primed
28.	Which of the following Output Equations determines the output of the State Machine?	MAX = Q0Q1EN
29.	When the transmission line is idle in an asynchronous transmission	It is set to logic high
30.	UVERPROM is stands for	Ultra-Voilet
31.	The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.	4
32.	Select the mode of programming in which GAL16V8 can be programmed:	All of the given
33.	The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.	CONSTATE
34	The domain of the expression AB'CD + AB' + C'D + B is	A, B, C and D
35.	The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.	Small
36.	_____ Counters as the name indicates are not triggered simultaneously.	Synchronous
37.	The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.	Three
38.	The output of a NAND gate is _____ when all the inputs are one.	Zero
39.	For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.	1

40.	A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.	True
41.	Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.	Shift Registers
42.	The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.	AND , OR
43.	A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:	1111
44.	Which of the following is a volatile memory?	DRAM
45.	The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.	REQ1
46.	The AND Gate performs a logical _____ function.	Division
47	Implementation of Latch is required almost _____ transistor.	Six
48.	Which one flip-flop has an invalid output state?	SR
49.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV 32
50.	The terminal count of a 4-bit binary counter in the UP mode is _____.	1100
51.	In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.	True
52.	The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.	Four
53.	Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.	RAM
54.	An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.	Q output of all flip-flops to clock input of next flip-flops
55.	In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.	D(OUT)
56.	Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.	256
57.	8-bit parallel data can be converted into serial data by using _____ multiplexer.	8-to-1
58.	If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.	1001
59.	Canonical form is a unique way of representing _____.	SOP

60.	A NOR based S-R latch is implemented using _____ gates instead of _____ gates.	NOR, NAND
61.	Cin is part of _____ Adder.	Full
62.	Flash memory Operation are classified into _____ different operation.	Two
63.	GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.	row, column
64.	In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.	7.8 microsec
65.	In the keyboard encoder, how many times per second does the ring counter scan the key board?	650 scans/second
66.	Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.	Negative-OR, Negative-AND
67	If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.	1
68.	The 64-cell array organized as 8 x 8 cell array is considered	as an 8 byte memory
69.	The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.	Synchronous
70.	PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.	PLDs
71.	For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.	None of the given
72.	A multiplexer with a register circuit converts	Parallel data to serial
73.	The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.	Four
74.	Which of the following Output Equations determines the output of the State Machine?	MAX = Q0Q1EN
75.	8-bit parallel data can be converted into serial data by using _____ multiplexer.	8-to-1
76.	You have to choose suitable option when your timer will reset by considering this given code: TRSTATE.CLK = clk; TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);	NSY2 or EWY2
77.	UVERPROM is stands for	Ultra-Voilet
78.	In memory write cycle, the time for which the WE signal remains active is known as the _____.	Write pulse width
79.	PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.	PLDs

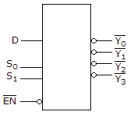
80.	The Transition table is very similar to the _____ table.	State
81.	Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.	Negative-OR, Negative-AND
82.	The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.	CONSTATE
83.	Adding two octal numbers "36" and "71" result in	127
84.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV 32
85.	A multiplexer with a register circuit converts	Parallel data to serial
86.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input
87.	Memory is arranged in _____.	two-dimensional manner
88.	Implementation of Latch is required almost _____ transistor.	Six
89.	In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.	D(OUT)
90.	Why demultiplexer is called a data distributor?	Single input to Single Output
91.	The maximum value, represented by a single hexadecimal digit is _____.	"F"
92.	Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.	RAM
93.	The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.	REQ1
94.	In a sequential circuit the next state is determined by _____ and _____	Current state and external input
95.	The divide-by-60 counter in digital clock is implemented by using two cascading counters:	Mod-6, Mod-10
96.	The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop	Hold time
97.	74HC163 has two enable input pins which are _____ and _____	ENP, ENT
98	_____ is said to occur when multiple internal variables change due to change in one input variable	Race condition
99.	The _____ input overrides the _____ input.	Asynchronous, synchronous
100.	A decade counter is _____.	Mod-10 counter

101.	In asynchronous transmission when the transmission line is idle, _____	It is set to logic high
102.	A Nibble consists of _____ bits.	4
103.	Excess-8 code assigns _____ to "-8"	0000
104.	The voltage gain of the Inverting Amplifier is given by the relation _____	Vout / Vin = – Rf / Ri
105.	LUT is acronym for _____	Look Up Table
106.	The three fundamental gates are _____	NOT, OR, AND
107.	The total amount of memory that is supported by any digital system depends upon _____	The size of the address bus of the microprocessor
108.	Stack is an acronym for_____	LIFO memory
109.	Addition of two octal numbers "36" and "71" results in _____	127
110.	._____ is invalid number of cells in a single group formed by the adjacent cells in K-map_____ is one of the examples of synchronous inputs.	J-K input
111.	_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	Clock Skew
112.	A GAL is essentially a _____.	Reprogrammable PAL
113.	_____, all the columns in the same row are either read or written.	FAST Mode Page Access
114.	In order to synchronize two devices that consume and produce data at different rates, we can use _____	Fist In First Out Memory
115.	A positive edge-triggered flip-flop changes its state when _____	Low-to-high transition of clock
116.	A frequency counter _____	Counts no. of clock pulses in 1 second
117.	In a sequential circuit the next state is determined by _____ and _____	Input and clock signal applied
118.	Given the state diagram of an up/down counter, we can find ____	The next state of a given present state
119.	The total amount of memory that is supported by any digital system depends upon _____	The size of the address bus of the microprocessor

120.	The expression F=A+B+C describes the operation of three bits _____ Gate.	OR
121.	The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.	32-bit
122.	The basic building block for a logical circuit is _____	A Logical Gate
123.	The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.	Zero
124.	_____ is invalid number of cells in a single group formed by the adjacent cells in K-map.	12

update answer if required

CS302 – GRAND QUIZ BY TEAM HADI

Sr No.	MCQS QUESTION	ANSWER
1.	(A+B).(A+C)=	A+BC
2.	Excess-8 code assigns _____ to "-8".	0000
3.	The output of the expression F=A.B.C will be logic _____ when A=1, B=0, C=1.	Zero
4.	The cell marked 6 in 4-variable K-Map represent minterm 6 or the maxterm 6 having the following binary value of variables A, B, C and D.	A=0, B=1, C=1, D=0
5.	A comparator circuit has multiple inputs and _____ outputs.	3
6.	The output A<B is set to 1 when the input combination is _____.	A=01, B=10
7.	The _____ encoder is used as keypad encoder.	Decimal-to-BCD Priority
8.	Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer.	A parallel to serial converter circuit
9.	The four outputs of two 4-input multiplexer, connected to form a 16-input multiplexer, are connected together through a 4-input _____ gate.	OR
10.	The device shown here is most likely a _____. 	Multiplexer
11.	GAL is acronym for _____.	Generic Array List
12.	In the binary number "10011" the weight of the most significant digit is _____.	2^4 (2 raise power 4)
13.	The output of the expression F=A+B+C will be logic _____ when A=0, B=1, C=1	10 (binary)
14.	Which of the following simplification method is intended to be used for Boolean expressions having more than four variables?	Quine-McCluskey
15.	A particular half-adder has _____ inputs and _____ output(s).	2, 2

16.	A quantity having continuous values is a/an _____ quantity.	Analog
17.	Which one of the following expressions is an example of Commutative Law of Multiplication?	AB+BA
18.	When four 1's are taken as a group of a Karnaugh map, the number of variables eliminated from the output expression is/are _____.	2
19.	Identify the Boolean expression that is in standard POS form.	$(A+\bar{B})(\bar{A}+B+\overline{C})$
20.	Simplifying POS (Product of Sum) expression requires the grouping of _____.	0s
21.	The decimal "17" in BCD will be represented as	10111
22.	A standard interface for programming the In-System PLD consists of _____.	4-wires
23.	_____ dual, 4-input multiplexer can be connected to form a 16-input multiplexer.	4
24.	S-R latch can be implemented using _____gates.	AND, OR
25.	A product term is 0 when _____.	Any of the literal is 0.
26.	What will be the output of a 3-input NAND Gate for the input values A=1, B=0, C=1	Zero
27.	_____ is not a valid hexadecimal number.	DEHF
28.	2's complement of any binary number can be calculate by	Adding 1 to 1's complement
29.	A BCD to 7-Segment decoder has _____ inputs and _____ outputs.	4, 7
30.	TTL based devices work with a DC supply of _____ Volts.	+5

31.	In CMOS 5 volt series, input voltage for logic high signal (V_{IH}) is in range of _____ volts.	3.5 to 5
32.	A multiplexer circuit has _____ inputs and _____ outputs.	Multiple , Multiple

update answer if required

CS302-GQ2020-SOLVED-BY-SONU-ILYAS-MUGHAL

Sr No.	MCQS QUESTION	ANSWER
1.	A _____ output can change from one state to the other by applying appropriate inputs.	Latch
2.	A function represented by an expression in _____ form can be readily programmed.	Standard SOP
3.	Portable devices that run on batteries use _____ circuit that have low power dissipation.	Integrated
4.	Removing the NOT gate at the output of the NOR gate results in an _____.	OR Gate
5.	The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or un-complemented B input to the connected to the Adder input.	AND, OR
6.	"The complement of a product of variables is equal to the sum of the complements of the variables." Is known as:	Demorgan's First Theorem
7.	The Boolean expression A+BC equals	(A+B)(A+C)
8.	If odd-parity is being used therefore the 4-bit data and the parity bit should add up to give _____ of 1s.	Odd
9.	The AND Gate performs a logical _____ function.	Multiplication
10.	_____ device dissipate varying amount of power depending upon the frequency of operation.	CMOS
11.	If the number if samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.	Different
12.	The Boolean expression (AB'CD') is _____.	A product term
13.	_____ methods are used to Convert Decimal Fractions to Binary.	2
14.	A.(B+C)=A.B+A.C is the expression of	Distributive Law
15.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input / Output
16.	Which of the following is the hexadecimal equivalent of 39?	27
17.	The product terms in Standard SOP are called?	Minterms
18.	A circuit that converts the n inputs to 2^n outputs is called	Decoder
19.	_____ is the example of Commutative Law of Multiplication.	AB+BA
20.	Each Octal Number digit can represent a _____ Binary number.	3-bit
21.	1011 – 101 = _____.	0110

22.	The output of the expression F=A.B.C will be logic _____ when A=1, B=0, C=1.	Zero
23.	In 32-bit Single-Precision Floating Point format representation the range of exponent value is from _____ to _____.	+127 to -126
24.	The _____ gate is used in applications where the output signal is a 1 when any one input is a 1.	OR
25.	Which of the following is the example of comparator?	XNOR
26.	A + B = B + A is _____.	Commutative Law
27.	+ is written in ABEL as _____.	#
28.	A 5-variable karnaugh map has	Thirty two cells
29.	1101 + 101 = _____.	10000
30.	Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.	256
31.	The series of TTL chips are characterized by their _____.	Switching Speed & Power Dissipation (Both)
32.	The 3-to-8 decoder has active-low outputs and three extra _____ gates connected at the three inputs to reduce the four unit load to a single unit load.	NOT
33.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input / Output
34.	A.(B+C)=A.B+A.C is the expression of _____.	Distributive Law
35.	GAL can be reprogrammed as instead of focuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.	Column, row
36.	NAND Gate is form by connecting _____.	AND Gate and then NOT Gate
37.	In 8-input multiplexer, the two outputs are connected through a/an _____ gate.	OR
38.	In 16-bit ALU, the Carry outputs C1, C2 and C3 from the look-Ahead Carry generator circuit are generated after a gate delay of _____.	2
39.	In 16-bit ALU, the G output is activated if the 4-bit generates a _____ irrespective of ___.	Carry out, carry in
40.	The sum term in Standard POS form are called _____.	Maxterms
41.	The limitation in implementation of parallel binary address is known as _____.	Carry propagation
42.	Gray Code of 8 is:	1100

43.	The output of an AND gate is one when _____.	All of the inputs are one
44.	Don't compare conditions are marked as _____ in the output column of the function table	X
45.	If a circuit suffers "Clock Skew" problem, the output of circuit can't be guaranteed.	True
46.	An Asynchronous down-counter is implemented (Using J-K flip-flop) by connecting _____.	Q' output of all flip-flops to clock input of next flip-flops
47.	If S=1 and R=0, then for positive edge triggered flip-flop Q(t+1)= _____.	1
48.	Flip flops are also called _____.	Bi-stable multivibrators
49.	The terminal count of a 4-bit binary counter in DOWN mode is _____.	0000
50.	The synchronous counters are also known as Ripple Counters _____.	False (Parallel Counters)
51.	The asynchronous counters are also known as _____.	Ripple Counters
52.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV-16
53.	If S=1 and R=0, then for negative edge triggered flip-flop Q(t+1)= _____.	Invalid
54.	In designing any counter the transition from a current state to the next state is determined by _____.	Current state and inputs
55.	In designing any synchronous counter a modulus number is used which determine the number of _____ used in counter.	Flip flops

update

CS302-GQ2020-SOLVED-BY-HACKER-GROUP

Sr No.	MCQS QUESTION	ANSWER
1.	A standard sum term is equal to _____ for only one combination of variable values.	Zero
2.	For all other variable values the standard sum term is equal to _____.	One
3.	The output A < B is set to 1 when the input combinations is	A=01, B=10
4.	Two 2-bit comparator circuits can be connected to form single 4-bit comparator	True
5.	High level Noise Margins (VNH) of CMOS 5 volt series circuits is	0.9V
6.	If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be	24.582
7.	The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol"+" here represents OR Gate.	One
8.	If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.	Reset
9.	3.3 v CMOS series is characterized by _____ and _____ as compared to the 5 v CMOS series.	Fast switching speeds, very low power dissipation
10.	The binary value "1010110" is equivalent to decimal _____.	86
11.	The _____ encoder is used as a keypad encoder.	Decimal to BCD Priority
12.	How many data select lines are required for selecting eight inputs?	3
13.	The Quad multiplexer has _____ outputs.	4
14.	Demultiplexer has	Single input and multiple outputs
15.	The expression _____ is an example of commutative law for multiplication.	AB = BA
16.	"Sum of weights" methods is used _____.	To convert from one number system to another
17.	A latch has _____ stable states.	Two
18.	Sequential circuits have storage elements	True

19.	The ABEL symbol for "XOR" operation is	$
20.	A demultiplexer is not available commercially.	True
21.	The main use of multiplexer is to	Select data from multiple sources and to route it to a single Destination
22.	The extended ASCII code is a _____ code.	8-bit
23.	The AND Gate performs a logical _____ function.	Multiplication
24.	The NOR Gate is formed by connecting _____.	AND Gate and then OR Gate
25.	Generally, the power dissipation of _____ devices remains constant throughout their operation.	TTL
26.	Two 2-bit comparator circuits can be connected to form single 4-bit comparator.	True
27.	When the control line in tri-state buffer is high the buffer operations like a _____ gate.	XOR
28.	The GAL22V10 has _____ inputs.	10
29.	The ABEL Symbol for "OR" operation is	#
30.	The ABEL Symbol for "NOT" operation is	!
31.	The ABEL Symbol for "AND" operation is	&
32.	The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10.	Similar with some enhancements
33.	All the ABEL equations must end with _____	; (semicolon)
34.	Circuit having a bubble at their outputs are considered to have an active-low outputs.	True
35.	$(A + B)(A + \bar{B} + C)(\bar{A} + C)$ is example of	Product of SUM
36.	Power consumption of TTL is higher than of _____.	CMOS
37.	Which device performs an operation which is the opposite of the decoder function?	Encoder Function
38.	The maximum number that can be represented using unsigned octal system is _____.	7
39.	The range of excess-8 code is from _____ to _____.	+7 to -8

CS302-GQ2020-RANDOM SOLUTION

Sr No.	MCQS QUESTION	ANSWER
1.	The look-ahead carry circuits ____.	Reduce propagation delay
2.	What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?	B'+C'D'=CD
3.	2-input, 8-bit multiplexer, by setting the S input to logic ____ the ____ inputs of both the multiplexer are selected.	High, B
4.	The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.	(2^64)-1
5.	When two or more product terms are summed by Boolean addition, the result is a _____ expression.	SOP
6.	Tri-state buffer is a _____ gate with a control line that disconnects the output from the input.	NOT
7.	The 4-bit 2's complement representation of "-7" is _____.	1001
8.	_____ and _____ are the steps of the Quine-McCluskey.	Find prime implicants , select minimal set of prime implicants.
9.	The binary number 1011, 101 has an integer part represented by ____ and a fraction part ___ separated by a decimal point.	1011, 101
10.	Subtractors also have output to check if 1 has been _____.	Borrowed
11.	CMOS technology is characterized by low power dissipation with ____ switching speeds.	Slow
12.	The _____ description is used to simulate the logic circuit and verify its operation.	Test vector
13.	How many outputs can an integrated circuit comparator have?	Three
14.	Which of the following is not the correct method of grouping?	Diagonally
15.	In the 32-bit single Precision floating point format, the exponent value ____ is reserved to represent infinity exponents.	99
16.	The output of XOR gate is zero (0) when	1. All the inputs are zero 2. All the inputs are one
17.	____ methods are used to convert decimal fractions to binary.	2
18.	To display the number ____ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD 7-Segment Display Digit.	29

19.	Both the multiplexer are selected simultaneously when ____ is set to logic ___ in 2-inputs, 8-bit multiplexer.	S, Low
20.	_____ function table are required to represent the input / output combination for each segment in 7-segment display.	7
21.	Multiplexer are also known as	Data Selectors
22.	The PLA can be programmed to give an output of constant _____ or _____.	0, 1
23.	Which of the following gates has the output 1 if and only if at least one input is 1?	OR
24.	The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through _____ ALU units in 16-bits ALU.	4 (Four)
25.	High Level Noise Margins (VNH) of CMOS 5 volt series circuits is _____.	0.9V
26.	Combinational logic is used for combinational circuits, where as Registered Logic is based on _____ circuits.	Sequential
27.	The OR Gate performs a Boolean _____ function.	Addition
28.	In 16-input multiplexer, the decoder inputs ____ and ___ enable one out of the four multiplexers.	C, D
29.	In CMOS 5 volt series, input voltage of logic high signal (VIH) with a ranges from ___ to ____ volts.	3.5, 5
30.	How many maximum group can be generated in 3 variable K map?	8
31.	Digital circuits operate with _____ voltage value(s).	2
32.	Which of the following is the octal equivalent of 28 decimal number?	34
33.	In cascading priority encoders, the EO output is connected to the EI input of the encoder which handles _____.	Lower priority outputs
34.	To determine the seven expressions for each of the seven outputs in 7-segment display, seven _____ variable Karnaugh maps are used.	4
35.	The output of NAND gate is _____ when all the inputs are one.	One
36.	The _____ is slowest and consumes more power.	Standard TTL
37.	The Boolean expression X=AB+CD represents	Two ANDs ORed together
38.	The expression F=A+B+C describes the operation of three bits _____ Gate.	OR
39.	Which of the following is NOT a valid rule of Boolean algebra? (Valid rules: A=1=1, AA=A, A=0=A)	A=A'
40.	_____ has the fastest switching speed and low power consumption.	Advanced low power Schottky
41.	Adjacent 1s detector circuit will have active high output for the input.	0011

42.	The PROM consists of a fixed non-programmable _____ gate array configured as a decoder.	AND
43.	Excess-8 code assigns _____ to "-8"	0000
44.	The 4-variable Karnaugh Map (K-Map) has _____ cells for min and max terms.	16
45.	Basic function of comparator is to _____ two binary quantities.	Compare
46.	The caveman number the value "2" is represented by symbol:	">"
47.	A circuit that converts the n inputs to 2^n outputs is called:	Decoder
48.	Adjacent 1s detector circuit will have active low output for the input.	1101
49.	_____ versions of logic gates are designed to withstand harsh and severe environmental conditions.	Military
50.	The Programmable Array Logic (PAL) has _____ AND array and a _____ OR array.	Programmable , fixed

CS302-GQ2020-RANDOM SOLUTION

Sr No.	MCQS QUESTION	ANSWER
1.	Divide-by-32 counter can be acheived by using	Flip-Flop and DIV 16
2.	The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)	(2 raise to power n)
3.	A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?	1001
4.	A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____	1111
5.	Divide-by-160 counter is acheived by using	DIV 16 and DIV 10
6.	A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.	8
7.	RCO stands for _____	Ripple Clock Output
8.	_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	Race condition
9.	Design of state diagram is one of many steps used to design	any counter
10.	An Astable multivibrator is known as a(n) _____	Oscillator

11.	The glitches due to "Race Condition" can be avoided by using a _____	Negative-Edge triggered flip-flops
12.	A decade counter is _____	Mod-10 counter
13.	The terminal count of a 4-bit binary counter in the DOWN mode is_____	0000
14.	_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	Clock Skew
15.	Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state	2
16.	In Synchronous systems, the output of all the digital circuits changes when an enable signal is applied instead of the clock signal.	False
17.	_____ flip-flops are obsolete now.	Master-Slave
18.	If the S and R inputs of the gated S-R latch are connected together using a _____ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)	NOT
19.	The glitches due to "Race Condition" can be avoided by using a _____	Negative-Edge triggered flip-flop Top of Form
20.	The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.	Hold Time
21.	We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using _____	J-K flip-flop
22.	The _____ input overrides the _____ input	Asynchronous, synchronous
23.	The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins	4
24.	_____ Counters as the name indicates are not triggered simultaneously Select correct option:	Asynchronous
25.	A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.	8