The 11-bit serial character format is shown. Figure 35.1.

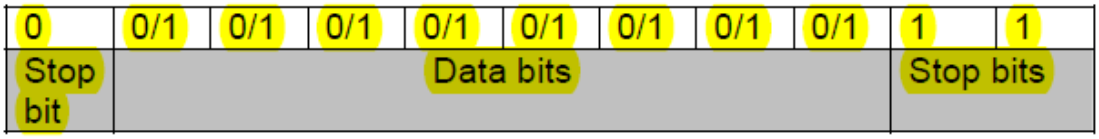


Figure 35.1 11-bit Serial Data format

Traffic Signal Controller Inputs and Outputs

The State Machine which controls the Traffic Signal has several inputs and outputs. The inputs are the

- NSSR: The NSSR is activated when a car is over either of the four sensors on the North-South section of the road
- EWSR: The EWSR is activated when a car is over either of the four sensors on the East-West section of the road

A Timer is used to count the 5 minute and 1 minute traffic signal cycle during the day and night. Two signals LTIME and STIME provide the timing inputs to the State Machine.

- LTIME: The LTIME signal is activated if 5 minutes have elapsed; the signal remains active unless the timer is reset.
- STIME: The STIME signal is activated if 1 minute has elapsed; the signal remains active unless the timer is reset.

The outputs of the State Machine are

- NSGrn: The Green signal controlling the traffic on the North-South section
- NSYel: The Yellow signal controlling the traffic on the North-South section
- NSRed: The Red signal controlling the traffic on the North-South section
- EWGrn: The Green signal controlling the traffic on the East-West section
- EWYel: The Yellow signal controlling the traffic on the East-West section
- EWRed: The Red signal controlling the traffic on the East-West section
- TMRST: The Reset signal which resets the timer after the LTIME or the STIME signals are activated to indicate a time interval of 5 and 1 minutes respectively.

State	NSGRN	NSYEL	NSRED	EWGRN	EWYEL	EWRED
NSG	on	off	off	off	off	on
NSY	off	on	off	off	off	on
NSY2	off	on	off	off	off	on
NSR	off	off	on	off	off	on
EWG	off	off	on	on	off	off
EWY	off	off	on	off	on	off
EWY2	off	off	on	off	on	off
EWR	off	off	on	off	off	on

Table 38.2b Switching of traffic lamps at different states

Memory Type	Non-Volatile	High Density	One-Transistor Cell	In-System Write ability
SRAM	No	No	No	Yes
DRAM	No	Yes	Yes	Yes
ROM	Yes	Yes	Yes	No
EPROM	Yes	Yes	Yes	No
EEPROM	Yes	No	No	Yes
FLASH	Yes	Yes	Yes	Yes

Table 42.1 A summary of Memory Types