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M.ABDULLAH

0344 2023 473

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Question No.1

In the highest frequency component in an analog signal is 20 KHz, what is the minimum sample frequency (Marks 2)

Answer:-

In the highest frequency component in an analog signal is 20 KHz, and minimum sample frequency is 40 KHz.

Question No.2

Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations. (Marks 2)

Answer:- Page 201

Logic Operation	ABEL Symbol
NOT	!
AND	&
OR	#
XOR	$

Question No.3

Differentiate between Moore machine and Mealy machine. (Marks 2)

Answer:- Page 318

The Sequential circuit whose output depends on the current state and the input is known as Mealy Machine.

Sequential circuit whose output is determined by the current state only is known as Moore Machine.

Question No.4

How many bytes will be there in 16K x 8 memory? (Marks 2)

Answer:- Page 395

A 16 K x 8 memory, stores 16K bytes or 16 x 1024 = 16384 bytes or 131072 bits.

Question No.5

How many address bits are required for a 2048-bit memory organized as a 256 x 8 memory? (Marks 3)

Question No.6

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Explain Rotate Right Operation of shift register with the help of Diagram. (Marks 3)

Answer:- Page 354

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The serial output of the register is connected to the serial input of the register. By applying clock pulses data is shifted right. The data shifted out of the serial out pin at the right hand side is re-circulated back into the shift register input at the left hand side. Thus the data is rotated right within the register.

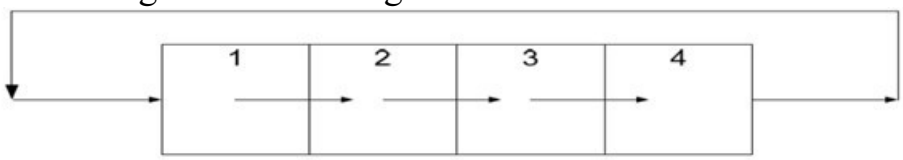


Figure 34.14 Rotate Right Operation

Question No.7

Difference between State Assignment and State Reduction process. (Marks 3)

Answer:- (Page 332 & 335)

1. In state Reduction A state diagram show the sequence of current and next states through which the state machine sequences while in State Assignment Each state in a sequential circuit is identified by a unique combination of binary bits.
2. In state Reduction the transition from a current state to the next state is determined by current state and the inputs while in State Assignment the states can be selected to allow minimum bit changes when changing from one state to the other.
3. State Assignment results in simpler combinational circuits that determine the next state while Reduction in the number of state results in fewer flip-flops and a simpler circuit.

Question No.8

Explain Full-Adder Sum and Carry out Boolean Expression. (Marks 3)

Answer:- (Page 135)

Full-Adder Sum & Carry Out Boolean Expressions

The Sum and Carry Out expressions of the Full-Adder can be determined from the function table. The Full-Adder Sum and Carry Out outputs are defined by the expressions

Sum = ABC + ABC + ABC + ABC

Sum = A(BC + BC) + A(BC + BC)

Sum = A(B ⊕ C) + A(B ⊕ C)

Sum = A ⊕ B ⊕ C

CarryOut = ABC + ABC + ABC + ABC

CarryOut = C(AB + AB) + AB(C + C)

CarryOut = C(A ⊕ B) + AB

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Question No.9

Explain Latches in your own words.(Marks 5)

Answer:- (Page 218)

A latch is a temporary storage device that has two stable states. A latch output can change from one state to the other by applying appropriate inputs. A latch normally has two inputs, the binary input combinations at the latch input allows the latch to change its state. A latch has two outputs Q and its complement Q(bar). The latch is said to be in logic high state when Q=1 and Q(bar)=0 and it is in the logic low state when Q=0 and Q(bar)=1. When the latch is set to a certain state it retains its state unless the inputs are changed to set the latch to a new state. Thus a latch is a memory element which is able to retain the information stored in it.

Question No.10

Differentiate between synchronous and asynchronous memory. (Marks 5)

Answer:- (Page 406)

In the Asynchronous memory the various input signals are asynchronous and are not tied to the clock, whereas in the Synchronous memory all the inputs are synchronized with respect to the clock and are latched into their various registers on an active clock pulse edge.

Question No.11

Draw state diagram of Moore machine.

(Marks 5) Answer:- (Page 338)

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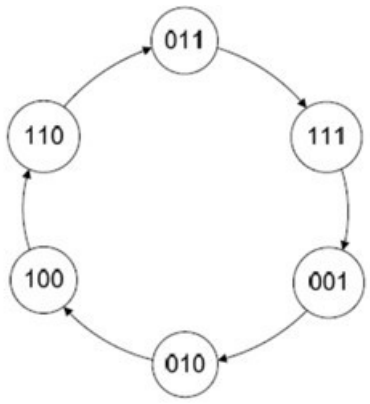


Figure 33.1 State diagram of a Moore Machine

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Question No:12 (Marks: 2)

Write down at least two applications of a shiftregister.

Answer:- (Page 356)

The two applications of the shift registers are

1. Serial to Parallel converter
2. Keyboard encoder

Question No:13 (Marks: 2)

Explain memory expansion process.

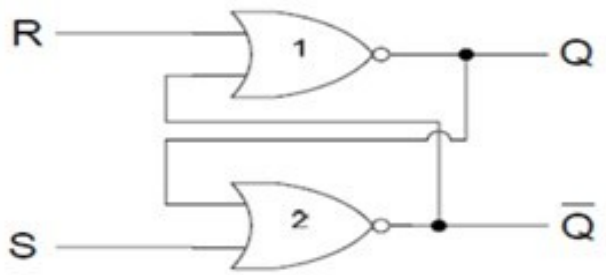
Answer:- (Page 430)

Computer and Digital systems have the capability to allow RAM memory to be expanded as the needed arises by inserting extra memory in dedicated memory sockets on the computer motherboard.

Question No:14 (Marks: 2)

Draw the NOR based S-R Latch

Answer:- (Page 220)



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Question No:15 (Marks: 3)

Explain Rotate Left Right Operation with the help of diagram.

Answer:- (Page 354)

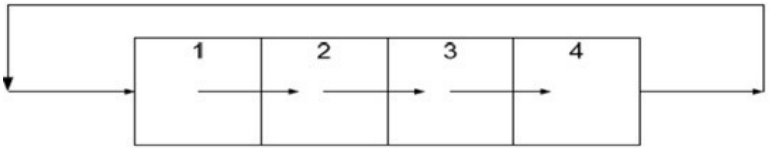


Figure 34.14 Rotate Right Operation

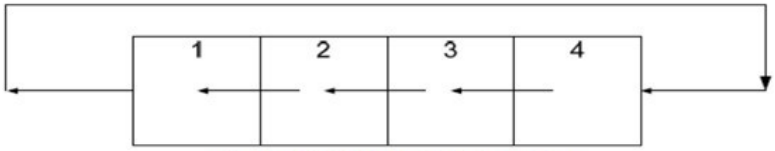
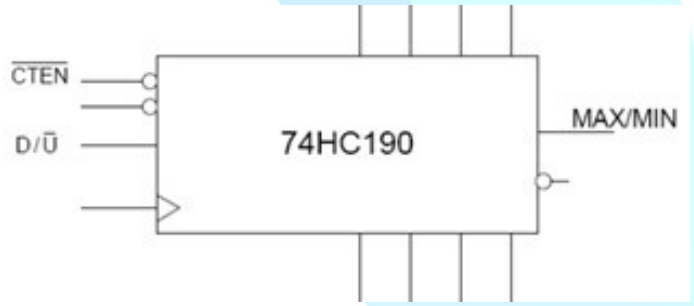


Figure 34.15 Rotate Left Operation

Question No:16 (Marks: 3)

You are given the block diagram of 74HC190 integrated circuit up/down counter, explain the function of labeled inputs/outputs.



Answer:-(Page 295)

1. Active-low CTEN counter enable input
2. D/U the count down/up input. When the input is set to logic 1, the counter counts down and when the input is set to logic 0, the counter counts up
3. The MAX/MIN output that is set to high when the terminal count 1001 is reached when counting up or when the terminal count 0000 is reached when counting down. The MAX/MIN output is logic high for one complete cycle when a terminal count is reached.

Question No:17 (Marks: 5)

Explain Memory Select or Enable Signals

Answer:- (Page 397)

In a computer system there are more than one memory chips to store program information. At any particular instant a read or write operation is carried out on a single addressable location. The unique location can only be accessed in one of the several memory chips, thus a single memory chip has to be selected before a read or write operation can be carried out. All

memory chips have a chip enable or chip select signal which has to be activated before the memory can be accessed.

Question No:18 (Marks: 5)

Explain the implementation of First In First Out (FIFO) Memory by using RAM.

Answer:- (Page 427)

Shift register based FIFO memory is used in digital systems designed for specific applications where small sized buffers are used to allow transfer of data between two devices operating at different data rates. Such digital systems either have no RAM or very small RAM for storing variables. Computers implement FIFO memory by reserving a part of their RAM memory for use as buffers. The Keyboard buffer for example is implemented by reserving a part of the RAM. When RAM is used as FIFO memory, two registers are used to point to the FIFO Buffer Out and Buffer In respectively. The two registers hold the addresses of the locations of the Buffer Out and Buffer In respectively, which are updated as new data is written into the buffer and previous data is read out from the FIFO buffer. Implementation of the FIFO buffer in RAM is usually takes the form of a circular buffer.

Question No:19 (Marks: 5)

Explain application of demultiplexer

Answer:- (Page 178)

Demultiplexer is used to connect a single source to multiple destinations. One use of the Demultiplexer is at the output of the ALU circuit. The output of the ALU has to be stored in one of the multiple registers or storage units. The Data input of the Demultiplexer is connected to the output of the ALU. Each output of the Demultiplexer is connected to each of the multiple registers. By selecting the appropriate output data from the ALU is routed to the appropriate register for storage.

The second use of the Demultiplexer is the reconstruction of Parallel Data from the incoming serial data stream. Serial data arrives at the Data input of the Demultiplexer at fixed time intervals. A counter attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored. When all the bits have been stored, data can be read out in parallel.

Question No: 20 (Marks: 2)

Explain the erase operation in context of Flash Memory.

Answer:- (Page 421)

During the erase operation charge is removed from the memory cell. A sufficiently large positive voltage is applied at the source with respect to the control gate. The voltage applied across the control gate and source is opposite to the voltage applied during programming. If charges are present on the gate, the positive voltage supply at the source attracts the electrons depleting the gate. A FLASH memory is erased prior to programming.

Question No.21

How can a serial in/parallel out register be used as a serial in/serial out register?

Question No.22

Explain the next-state table with the help of a table for any sequential circuit?

Answer:- (Page 306)

Once the state diagram of the sequential circuit is defined, a Next-State Table is derived which lists each present state and the corresponding next state. The next state is the state to which the sequential circuit switches when a clock transition occurs.

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Question No.23

What is meant by Non-Monotonicity of Digital to Analog converter?

Answer:- (Page 460)

if the D/A converter outputs a lower voltage than its preceding output voltage the converter is said to exhibit non-monotonic behavior.

Question No.24

Write down at least two functions of a register.

Answer:- (Page 306)

Technically, a register performs two basic functions. It stores data and it moves or shifts data. The shifting of data involves shifting of bits from one flip-flop to the other within the register or moving data in and out of the register. The shift operation of the binary data is carried out by applying clock signals. Several different kinds of shift operations can be identified.

Question No.25

You are given the Next-state table of a Moore machine, using this information draw the state diagram of the machine.

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	1	1	1	1	1
1	1	1	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	1	0
1	1	0	0	1	1

Answer:-(Page 338)

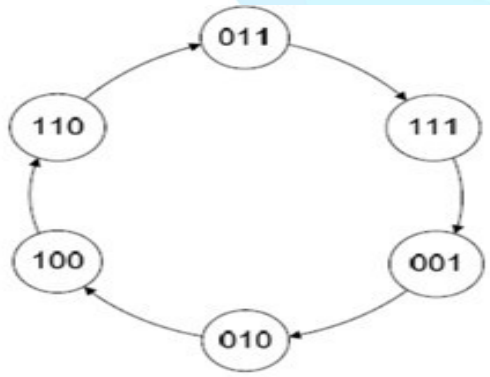


Figure 33.1 State diagram of a Moore Machine

Question No.26

Define the term "Variable" in context of Boolean algebra.

Answer:- (Page 71)

A variable is a symbol usually an uppercase letter used to represent a logical quantity.

A variable can have a 0 or 1 value.

Question No.27

A general sequential circuit consists of a combinational circuit and memory elements. How this Memory element is implemented.

Answer:- (Page 318)

A general Sequential circuit consists of a combinational circuit and a memory element. The memory element is made of a set of n flip-flops all connected to a a common clock. The n flip flops store 2n states. The flip-flops change their current state to the next state on each clock transition. The next state is determined by the current state and the external input. The output of the State Machine is determined by the current state and external input. The inputs to the memory which allow the memory to change its state on a clock transition are known as excitation inputs or excitation variables.

Question No.28

what is meant by Monotonicity of Digital to Analog converter?

Answer:- (Page 460)

The output of the D/A converter should give an increasing analogue voltage output when the binary input is varied between its minimum and maximum values.

Question No.29

Explain Programmable Logic Devices?

Answer:-(Page 179)

Programmable Logic Devices are used in many applications to replace the Logic gates and MSI chips. PLDs save circuit space and reduce and save the cost of components in a Digital Circuit. PLDS consists of Arrays of AND gates and OR gates that can be programmed to perform specific functions.

Question No.30

How many clock pulses are required to enter a byte of data serially into an 8-bit shift register? 2 Answer:-

8 clock pulses are required to enter a byte of data serially into an 8- bit shift register

Question No.31

How can calculate the frequency of an unknown signal?

Answer:-(Page 301)

The frequency of the unknown signal can be calculated by counting the number of clock pulses of the unknown signal and dividing the count number by the time interval in which the clock pulses are counted,

Question No.32

Write the drawbacks of 16-bit ALU without look-Ahead carry circuit?

Question No.33

How many address bit are required for a 2048-bit memory organized as a 256*8 memory?

Question No.34

Differentiates between Memory capacity and Memory Density?

Answer:- (Page 395)

Each memory array has a maximum capacity to store information in the form of bits. Memory density on the other hand specifies the number of bits stored per unit area. More the number of bits stored in a unit area more dense the memory, that is, more bits are stored in less space.

Question No.35

Explain Memory Select or Enable signal?

Answer:- (Page 397)

In a computer system there are more than one memory chips to store program information. At any particular instant a read or write operation is carried out on a single addressable location. The unique location can only be accessed in one of the several memory chips, thus a single memory chip has to be selected before a read or write operation can be carried out. All memory chips have a chip enable or chip select signal which has to be activated before the memory can be accessed.

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Question No.36

Explain state Assignment Process.

Answer:-(Page 335)

Each state in a sequential circuit is identified by a unique combination of binary bits. Unless the output of the sequential is directly taken form the flip-flop outputs such as counters, the states can be selected to allow minimum bit changes when changing from one state to the other. Keeping the bits changes to minimum when changing from one state to the next, results in simpler combinational circuits that determine the next state.

Question No: 37 (Marks: 2)

Some of the counters (e.g. 74HC163) are called pre-set counters. why?

Answer:-

74HC163) are called pre-set counters because A counter set in advance to stop or produce output once a specific count has been reached.

Question No: 38 (Marks: 2)

How many bytes will be there in 32 K x 8 memory?

Answer:- (Page 395)

A 32 K x 4 memory stores 32K nibbles or 32 x 1024 = 32768 nibbles

Question No: 39 (Marks: 3)

Differentiate between truth table and next-state table.

Question No.40

Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State assignment 1	State assignment 2
A	00	00
B	01	01
C	11	10
D	10	11

Question No.41

Convert the hexadecimal number 7AB1 into binary numbers. Write down all the steps. **Answer:- (Page 27)**

Replacing each Hexadecimal digit by its 4-bit binary equivalent
7= 0111, A= 1010, B=1011, 1= 0001 So, 7AB1 = 0111101010110001

Question No.42

Explain grouping of cells in k-map. **Answer:- (Page 90)**

Groups are formed on the basis of 1s (Minterms) or 0s (maxterms). A group is selected to have maximum number of cells of Minterms or Maxterms, keeping in view that the size of the group should be a power of 2. The idea is to form minimal number of largest groups that uniquely cover all the cells, thereby ensuring that all minterms or maxterms are included.

Question No.43

Provide some of guidelines for selection of state assignment. 3

Answer:-

- Choose an initial coded state into which the state machine (sequential circuit) can easily be forced to reset (000 or 111)
- Minimize the State Variables that change on each transition
- Maximize the number of state variables that don't change in a group of related states
- If there are unused states, then choose the best state variable combinations to achieve the first three goals.

Question No.44

Discuss at least one difference in Johnson and ring Counter

Answer:-(Page 355)

The Ring Counter is similar to the Johnson counter, except that the Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

Question No.45

Three types of error while converting Analogue signal into digital

Answer:

1. Missing Code
2. Incorrect Code
3. Offset Error

Question No.46

Explain memory read operation with help of example 5

Answer:- (page 397)

Memory Read operation is carried out by first selecting the memory chip by activating the Memory Select signal. The Read signal is asserted to configure the memory circuitry for reading data from the memory. An address (100) is applied on the Address Lines. The internal address decoder of the memory decodes the address and selects one unique row from which data is read. Figure 39.4.

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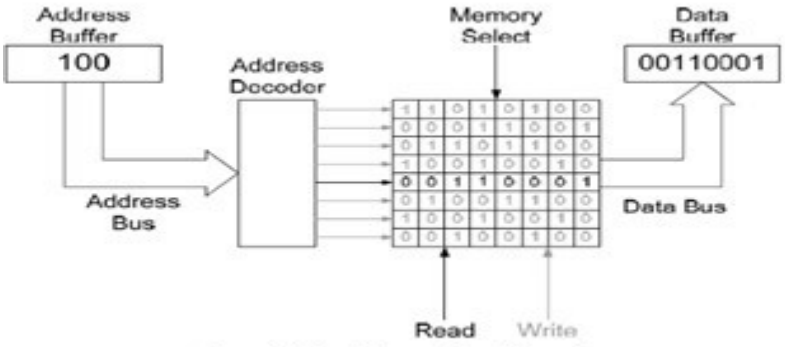


Figure 39.4 Memory Read Operation

The address of the location in the memory from which data is to be read is supplied by the microprocessor. The microprocessor stores the address in its address buffer. The data read from the memory is stored in a data buffer inside the microprocessor. In the diagram shown, a microprocessor places an address 100 on its external address bus connected to the address lines of the memory. The internal address decoder of the memory decodes the address 100 and activates a row select line which selects the row location 4. The data (00110001) at the location is read from the memory and placed on the data bus where it is latched by the microprocessor and stored in its data buffer.

Question No.47

Explain flesh analogue to digital converter. marks 5

Answer:- (Page 447)

The Flash A/D converter is based on a resistor potential divider, where multiple resistors of identical value form a voltage divider. A reference voltage is applied at one end of the potential divider which divides the voltage equally across all the resistors. The input analogue voltage is applied at the non-inverting inputs of a set of Op-Amp based comparators. The inverting input of each comparator is connected to the resistive voltage divider which provides reference voltages for all the comparators. If the input voltage is larger than the reference voltage the output of the comparator is logic high otherwise it is logic low. The outputs of all the comparators are connected to the input of a priority encoder which converts the comparator outputs to a binary coded equivalent value.

Question No.48

Briefly explain address multiplexing in DRAM. marks5

Answer:- (Page 410)

DRAM chips use address multiplexing to reduce the number of address lines by half. The address required to select a memory location is split into row and column addresses. To access a DRAM location for reading or writing of information the row address is first applied at the

address lines. The row address is latched by the Row Address Latch of the DRAM memory chip. The column address is applied next at the same address lines. The column address is latched by the Column Address Latch. Two signals RAS and CAS are used as strobe signals to control the Row Address and Column Address latches respectively. The external address lines are multiplexed as the same set of address lines are used to apply the row address and the column address at different time instances. The outputs of the Row Address Latch and the Column Address Latch are connected to the Row and Column Decoders which select a single row and column line selecting the storage cell to be accessed.

Question No.49

Explain READ Write signal used for memory. Marks 3

Answer:- (Page 396)

Read/Write signals are required to configure the memory for read and write operation. Memory chips have a single Read/Write signal. When the signal is set to high it allows data to be read from the memory. When the signal is set to low data is written into the memory. Some memory chips have two separate Read and Write signals. The read and write signals are separately asserted to control the Read and Write operation.

Question No.50

What is difference between PROM and ROM. Marks 3

Answer:-

The difference between a PROM and a ROM (**r**ead-**o**nly **m**emory) is that a PROM is manufactured as blank memory, whereas a ROM is programmed during the manufacturing process. To write data onto a PROM chip, you need a special device called a PROM programmer or PROM burner. The process of programming a PROM is sometimes called burning the PROM.

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Question No.51

Making decade counter by cascading two 74HC163. 05

Question No.52

Explain don‟s care condition.

Answer:- (Page 96)

Function Tables represent the function by listing all the possible inputs and marking the corresponding outputs with 1s and 0s. Thus a circuit having four inputs can be described by a 4-variable function table having 16 possible input combinations. For each of the 16 possible

input conditions the corresponding output bits are marked as 1s and 0s depending upon the minterms or maxterms. It is however, possible that out of the 16 possible input combinations, three input combinations never occur. Since these three input combinations never occur so should their corresponding outputs be marked as 0s or 1s? Since these inputs never care therefore we don't need to worry about the output of these input states. They are considered to be don't care conditions.

Question No: 53 (Marks: 5)

Performance characteristics of D/A converters are determined by five parameters. Name them.

Answer:- (Page 460)

Performances characteristics of D/A converters are determined by five parameters are:
1. Resolution 2. Linearity 3. Monotonicity 4. Setting time 5. Accuracy

Question No.54

Give advantages of Counters are available in integrated circuits? (Marks 2)

Question No.55

Successive approximation counter have a fixed consecutive time Is tarha ka qs tha (Marks 2)

Question No.56

How many states in 8-bit Johnson counter? (Marks 2)

Answer:-(Page 354)

The sequence of states that are implemented by a n-bit Johnson counter are 2n So, 8 bit Johnson counter has 2*8 = 16 states

Question No.57

Diff b/w truth table and next state table (Marks 3)

Question No.58

How hexadecimal number is converted into binary number give one example? (Marks 3)

Answer:-(Page 28)

Converting from Hexadecimal back to binary is also very simple. Each digit of the Hexadecimal number is replaced by an equivalent binary string of 4-bits. FD13 Hexadecimal Number 1111 1101 0001 0011 Replacing each Hexadecimal digit by its 4-bit binary equivalent

Programmable Logic Devices are based on a programmable AND-OR gate array which are programmed to implement any function in the SOP form. The output of the AND-OR gate array can be directly used as a combinational circuit output. Provision is there to connect the output of the AND-OR gate array to a D-flip-flop for Sequential circuit operation. An FPGA is a more flexible device than PLDs as instead of a single AND-OR gate array, an FPGA device contains multiple logic blocks that can be individually programmed to perform different functions. Each Logic Block is connected to other blocks through row and column interconnects that can be programmed to connect any Logic block to another.

Question No: 59 (Marks: 5)

Differentiate between synchronous and asynchronous RAM.

Answer:- (Page 406)

Synchronous RAM is very similar to the Asynchronous RAM, in terms of the memory array, the address decoders, read/write and enable inputs. In the Asynchronous memory the various input signals are asynchronous and are not tied to the clock, whereas in the Synchronous memory all the inputs are synchronized with respect to the clock and are latched into their various registers on an active clock pulse edge.

Question No: 60 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

Answer:- (Page 222)

Input		Output
S	R	Qt+1
0	0	Q_t
0	1	0
1	0	1
1	1	invalid

Table 22.3 Truth-Table of NOR based S-R Latch

Question No: 61 (Marks: 2)

Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State Assignment 1	State Assignment 1
A	00	00

B	01	01
C	11	10
D	10	11

Question No: 62 (Marks: 3)

Given the following statement used in PLD programming:
Y PIN 23 ISTYPE „com";
Explain what does this statement mean?

Answer:- (Page 360)

The statement describes Y available at output pins 23. The Y variable is a 'Combinational' output available directly from the AND-OR gate array output. The active-low or active-high output of the Registered Mode can also be specified in the declaration statement

Question No: 63 (Marks: 3)

Explain dynamic RAM in your own words.

Answer:-

Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory.

Question No.64 (Mark s: 2)

Define quantization process.

Answer:- (Page 444)

The process of converting the analogue signal into a digital representation (code) is known as quantization

Question No.65 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer and 2-to-4 Binary Decoder?

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Answer:- (Page 178)

The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure 16.10. Assuming the select inputs I1 and I0 are set to 1 and 0 respectively. The O2 output is set to 1 if the Data input is 1 or it is set to 0 if the Data input is 0.

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CS302 Quiz 2

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Whatsapp Group:https://chat.whatsapp.com/BEliqpKfBH1CNShjqxSkb4

If the height of perfect binary tree is 4, what willbe the total number of nodes in it?

31

Suppose there are set of fruits and the set ofvegetables, both sets are_____sets.

Disjoint

A binary relation R over S is called an equivalencerelation if it has following property(s)

All of Above

Heap can be used to implement

Priority queue

If a tree has 20 edges/links, then the total numberof nodes in the tree will be:

21

If there are 100 elements in an equivalence class,then we will have sets initially.

100

Given the values are the array representation of heap; 12 23 26 31 34 44 56 64 78 100 What is the5th smallest element in the given heap?

34

A solution is said to be efficient if it solves theproblem within its resource constraints i.e. hardware and time.

True

Which one of the following is known as "Last-In,First-Out" or LIFO Data Structure?

Stack

What will be postfix expression of the followinginfix expression? infix Expression: a+b*c-d

abc*+d-

For compiler a postfix expression is easier toevaluate than infix expression?

True

Consider the following pseudo code declare astack of characters while (there are more characters in the word to read)

{

read a character

push the character on the stack

}

while (the stack is not empty)

{

pop a character off the stack write the character to the screen

}

What is written to the screen for the input"apples"?

selppa

A binary tree of N nodes has .

Log2 N levels

The easiest case of deleting a node from BST isthe case in which the node to be deleted .

Is a leaf node

If there are N elements in an array then the numberof maximum steps needed to find an element usingBinary Search is .

log2N

Merge sort and quick sort both fall into the samecategory of sorting algorithms. What is this category?

None of the given options.

If one pointer of the node in a binary tree is NULLthen it will be a/an .

External node

We convert the _ pointers of binary to threads inthreaded binary tree.

NULL

If the bottom level of a binary tree is NOT completely filled, depicts that the tree is NOT

complete Binary tree

What is the best definition of a collision in a hashtable?

Two entries with different keys have the sameexact hash value.

Suppose that a selection sort of 100 items has completed 42 iterations of the main loop. How many items are now guaranteed to be in their finalspot (never to be moved again)

42

Suppose you implement a Min heap (with the smallest element on top) in an array. Consider thedifferent arrays below; determine the one that cannot possibly be a heap:

16, 24, 20, 30, 28, 18, 22

Do you see any problem in the code ofnextInOrder

below: TreeNode * nextInorder(TreeNode * p)

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```
{
if(p->RTH == thread)return( p->R );
else {
p = p->R;

while(p->LTH == child)p = p->R;
return p;

}

}
```

The function has logical problem, therefore, it willnot work properly.

Here is an array of ten integers: 5 3 8 9 1 7 0 2 6 4The array after the FIRST iteration of the large loop in a selection sort (sorting from smallest to largest).

0 3 8 9 1 7 5 2 6 4

Which one of the following operations returns topvalue of the stack?

Top

Which one of the following is NOT true regardingthe skip list?

List Sh contains only the n special keys.

By using we avoid the recursive method of traversing a Tree, which makes use of stacks andconsumes a lot of memory and time.

Threaded binary tree

What is the best definition of a collision in a hashtable?

Two entries with different keys have the sameexact hash value.

Which formula is the best approximation for thedepth of a heap with n nodes?

log (base 2) of n

which of the following is not true regarding themaze generation?

Remove a randomly chosen wall if the cells itseparates are already in the same set.

Which of the given option is NOT a factor inUnion by Size:

Make the larger tree, the subtree of the smallerone.

when we have declared the size of the array, it is not possible to increase or decrease it during the ofthe program.

Execution

it will be efficient to place stack elements at the start of the list because insertion and removal taketime.

Constant

is the stack characteristic but was implementedbecause of the size limitation of the array.

isEmpty() , isFull()

What kind of list is best to answer questions suchas "What is the item at position n?"

Lists implemented with an array.Each node in doubly link list has,

2 pointers

If there are 56 internal nodes in a binary tree thenhow many external nodes this binary tree will have?

57

A simple sorting algorithm like selection sort or bubble sort has a worst-case of O(n2) time becausesorting 1 element takes O(n) time - After 1 pass through the list, either of these

algorithms can guarantee that 1 element is sorted.

Merge sort and quick sort both fall into the samecategory of sorting algorithms. What is this category?

None of the given options.

Huffman encoding uses tree to develop codes of varying lengths for the letters used in the originalmessage.

Binary tree

Consider a min heap, represented by the followingarray: 10,30,20,70,40,50,80,60 Afer inserting a node with value 31.Which of the following is the updated min heap?

10,30,20,31,40,50,80,60,70

Consider a min heap, represented by the followingarray: 11,22,33,44,55 After inserting a node with value 66.Which of the following is the updated min heap?

11,22,33,44,55,66

Suppose that a selection sort of 100 items has completed 42 iterations of the main loop. How many items are now guaranteed to be in their finalspot (never to be moved again)?

42

Is a data structure that can grow easily dynamically at run time without having to copy existing elements.

Both of these

A complete binary tree of height has nodesbetween 16 to 31 .

4

Which of the given option is NOT a factor inUnion by Size:

Make the larger tree, the subtree of the smallerone.

Here is an array of ten integers:

5 3 8 9 1 7 0 2 6 4

The array after the FIRST iteration of the large loop in a selection sort (sorting from smallest tolargest).

0 3 8 9 1 7 5 2 6 4

Suppose A is an array containing numbers in increasing order, but some numbers occur more than once when using a binary search for a value,the binary search always finds

the first occurrence of a value.

A binary tree with 24 internal nodes has externalnodes. 22

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25

77.it will be efficient to place stack elements at thestart of the list because insertion and removal take time.

Constant

“+” is a operator.

Binary

A kind of expressions where the operator is present between two operands called expressions.

Infix

Here is a small function definition:void f(int i, int &k)

{

i = 1;

k = 2;

}

Suppose that a main program has two integer variables x and y, which are given the value 0. Then the main program calls f(x,y); What are thevalues of x and y after the function f finishes?

x is still 0, but y is now 2.

A binary tree with N internal nodes has links, linksto internal nodes and links to external nodes

2N, N-1, N+1

Each node in doubly link list has,

2 pointers

If you know the size of the data structure in advance, i.e., at compile time, which one of thefollowing is a good data structure to use.

Both of these

Which one is a self-referential data type?Link list

There is/are case/s for rotation in an AVL tree,

4

Which of the following can be the inclusioncriteria for pixels in image segmentation.

All of the given options

In a perfectly balanced tree the insertion of a nodeneeds .

One rotation

If there are N elements in an array then the number of maximum steps needed to find anelement using Binary Search is .

log2N

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Which of the following is NOT a correct statementabout Table ADT?

A table consists of several columns, known asentities.

Suppose we are sorting an array of eight integers using quick sort, and we have just finished the first partitioning with the array looking like this:

2 5 1 7 9 12 11 10

Which statement is correct?

The pivot could be either the 7 or the 9

What is the best definition of a collision in a hashtable?

Two entries with different keys have the sameexact hash value.

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Cs302 Quiz no 2

To write data to the memory the memory the write cycle is initiated by

Applying the address signals

The counter states or the range of the number of a counter is determined by the formula(“n” represented the total number of flip-flops)

2 raise to power n

THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT_____GATE

OR

A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BYTHE MANUFACTURER.

TRUE

in sequential circuits memory elements are connected with_____.

common clock

A synchronous decade counter will have_____flip-flops

4

the terminal count of a modulus -13 binary counter is

1101

The alternate solution for a multiplexer and a register circuit is _____

Parallel in / Serial out shift register

A 8-bit serial in / parallel out shift register contains the value “8”,_____clock signal(s) will be required to shift the value completely out of the register.

8

Which of the following output equations determines the output of the state machine?

Max-Q0Q1EN

The CONSTATE.CLK = Clock is used to indicate that the_____state variables change on a clock transition.

CONSTATE

Memory is arranged in_____.

two-dimensional manner

The n flip-flops store_____states.

2^n

PALs tend to execute_____logic.

SOP

In DRAM read cycle R /W- signal is activated to read data which is made available on the_____data line.

D(OUT)

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A SOP expression can be implemented by an_____combination of gates.

AND-OR

Why demultiplexer is called a data distributor?

Single input to Single Output

If the number of samples that are collected is reduced by half, the reconstructed signal will be_____from/to the original.

Same

The AND Gate performs a logical_____function.

Division

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

_____is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The 64-cell array organized as 8 x 8 cell array is considered

as an 8 byte memory

A 3-variable karnaugh map has

eight cells

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_____Counters as the name indicates are not triggered simultaneously.

Synchronous

The ABEL Input file can use a_____instead of the equation to specify the Boolean expressions.

Truth Table

The_____gate and_____gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

Flash memory Operation are classified into_____different operation.

Two

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A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

AND

The domain of the expression AB'CD + AB' + C'D + B is

A, B, C and D

The Adjacent 1s Detector accepts 4-bit inputs. If_____adjacents 1s are detected in the input, the output is set to high.

1

Which of the following Output Equations determines the output of the State Machine?

MAX = Q0Q1EN

When the transmission line is idle in an asynchronous transmission

It is set to logic high

In NAND based S-R latch, output of each_____gate is connected to the input of the other_____gate.

NAND, NAND

PLDs have In-System Programming (ISP) capability that allows the_____to be programmed after they have been installed on a circuit board.

PLDs

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The terminal count of a 4-bit binary counter in the UP mode is_____.

1100

Select the mode of programming in which GAL16V8 can be programmed:

All of the given

Consider the sum of weight method for converting decimal into binary value,

_____is the highest weight for 411.

256

If two numbers in BCD representation generate an invalid BCD number then the binary_____is added to the result.

1001

In memory write cycle, the time for which the WE signal remains active is known as the_____.

Write pulse width

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a_____with a_____.

row, column

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The S-R latch has two inputs, therefore_____different combinations of inputs can be applied to control the operation of the S-R latch.

four

The Transition table is very similar to the_____table.

State

A NOR based S-R latch is implemented using_____gates instead of _____ gates.

NOR, NAND

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using_____.

Shift Registers

For a down counter that counts from (111 to 000), if current state is "101" the next state will be_____.

None of the given

The NOR logic gate is the same as the operation of the_____gate with an inverter connected to the output.

NAND

The ROM used by a computer is relatively_____as it stores few byres of code used to Boot the Computer system on power up.

Small

Canonical form is a unique way of representing_____.

SOP

UVERPROM is stands for

Ultra-Voilet

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If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a_____.

1

Cin is part of_____Adder.

Full

Which one flip-flop has an invalid output state?

SR

Which of the following is a volatile memory?

DRAM

The maximum value, represented by a single hexadecimal digit is_____.

"F"

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack_____.

Top

8-bit parallel data can be converted into serial data by using_____multiplexer.

8-to-1

You have to choose suitable option when your timer will reset by considering this given code:

TRSTATE.CLK = clk;

TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

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NSY2 or EWY2

The FAST Model Page Access allows_____memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

Adding two octal numbers "36" and "71" result in_____.

127

The Static Ram (SRAM) is non-volatile and is not a_____density memory as a latch is required to store a single bit of information.

High

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and_____gates respectively.

Negative-OR, Negative-AND

A multiplexer with a register circuit converts

Parallel data to serial

Implementation of Latch is required almost_____transistor.

Six

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____inputs.

Synchronous

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to_____location(s) using a single address.

Four

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be_____.

One

The 74HC163 is a 4-bit Synchronous counter, it has_____data output pins.

4

The_____input overrides the_____input.

Asynchronous, synchronous

The Test Vector definition defines the test vectors for all the three counter inputs and_____counter output/outputs.

Three

Subtractors also have output to check if 1 has been_____.

Primed

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting_____.

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Q output of all flip-flops to clock input of next flip-flops

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 32

For a Standard SOP expression, a_____is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Two signals_____and_____provide the timing inputs to the State Machine.

PTIME and QTIME

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

-WE

Implementation of the FIFO buffer in_____is usually takes the form of a circular buffer.

RAM

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in_____when Distributed refresh is used.

7.8 microsec

The output of a NAND gate is_____when all the inputs are one.

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Zero

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires_____gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------

THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

The terminal count of a 4-bit binary counter in the UP mode is .

1111

For a down counter that counts from (111 to 000). If current state is “101” the next state will be

110

The n flip-flops store states.

2^n

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting

Q output of all flip-flops to clock input of next flip-flops

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated. Circuit counters allow cascading of multiple counters together.

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True

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

False

The 74HC163 is a 4-bit Synchronous Counter, it has data output pins.

4

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 16

The synchronous counters are also known as Ripple Counters:

False

Each stage of Master-slave flip-flop works at of the clock signal

One half

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

80 micro seconds

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Number of states in an 8-bit Johnson counter sequence are:

16

In moore machine the output depends on

The current state

Asynchronous mean that

Each flip-flop after the first one is enabled by the output of the preceding flip-flop

According to moore circuit, the output of synchronous sequential circuit depend/s on of flip flop.

Present state

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

0

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

A one-shot mono-stable device contains _

NOR gate, Resistor, Capacitor and NOT Gate

The inputs can be directly mapped to karnaugh maps.

J-K

A mono-stable device only has a single stable state

True

When the Hz sampling interval is selected, the signal at the output of the J-K flipflop has a time period of seconds.

1, 2

The_____Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

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3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

1

NOR gate is formed by connecting _____

OR Gate and then NOT Gate

A particular half adder has

2 INPUTS AND 2 OUTPUT

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .

Toggle

A stage in the shift register consists of

A flip flop

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If a circuit suffers “Clock Skew” problem, the output of circuit can’t be guarantied.

True

A modulus-14 counter has fourteen states requiring

4 flip flops

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

NOT

flip-flops are obsolete now.

Master-Slave

The glitches due to “Race Condition” can be avoided by using a .

Negative-Edge triggered flipflops

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=

1

occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock skew

An Astable multivibrator is known as a (n) .

Oscillator

In Master-Slave flip-flop setup, the master flip-flop operators at

Both Master-Slave operator simultaneously

The power consumed by a flip-flop is defined by _

c.P = Vcc x Icc

The 3-bit up counter can be implemented using flip-flop(s).

S-R flip-flops and D-flip-flops

The terminal count of a 4-bit binary counter in the DOWN mode is

0000

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If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

NOT

The low to high or high to low transition of the clock is considered to be a(n) _____

Edge

RCO Stands for _____

Ripple Clock Output

A transparent mode means _____

The changes in the data at the inputs of the latch are seen at the output

In_____outputs depend only on the current state.

Moore Machine

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Smallest unit of binary data is a _____

Bit

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

State assignment

State of flip-flop can be switched by changing its

Input signal

Once the state diagram is drawn for any sequential circuit the next step is to draw

Next-state table

Design of state diagram is one of many steps used to design

A truncated counter

Flip flops are also called_____.

Bi-stable multivibrators

Three cascaded modulus-10 counters have an overall modulus of

1000

The term hold always means .

No change

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

J=X(Don’tcare),K=0

To parallel load a byte of data into a shift register, there must be

One clock pulse

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Invalid state of NOR based SR latch occurs when_____.

S=1, R=1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called_____of the flip-flop.

Hold time

74HC163 has two enable input pins which are_____and _____

ENP, ENT

_____is said to occur when multiple internal variables change due to change in one input variable

Race condition

The_____input overrides the_____input

Asynchronous, synchronous

A decade counter is_____.

Mod-10 counter

In asynchronous transmission when the transmission line is idle, _____

It is set to logic high

A 8-bit serial in / parallel out shift register contains the value “8”,_____clock signal(s) will be required to shift the value completely out of the register.

8

In a sequential circuit the next state is determined by_____and _____

Current state and external input

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

Mod-6, Mod-10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

True

A Nibble consists of_____bits

4

Excess-8 code assigns_____to "-8"

0000

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

LUT is acronym for _____

Look Up Table

The three fundamental gates are _____

NOT, OR, AND

The total amount of memory that is supported by any digital system depends upon _____

The size of the address bus of the microprocessor

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Stack is an acronym for _____

LIFO memory

Addition of two octal numbers “36” and “71” results in _____

127

_____is one of the examples of synchronous inputs.

J-K input

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock Skew

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____is used to simplify the circuit that determines the next state.

State assignment

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

0000

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

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Doesn’t have an invalid state

A multiplexer with a register circuit converts _____

Parallel data to serial

GAL is essentially a_____.

Reprogrammable PAL

in_____, all the columns in the same row are either read or written.

FAST Mode Page Access

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Fist In First Out Memory

A flip-flop changes its state when _____

Low-to-high transition of clock

A frequency counter _____

Counts no. of clock pulses in 1 second

In a sequential circuit the next state is determined by_____and _____

Input and clock signal applied

Flip flops are also called _____

Bi-stable multivibrators

Given the state diagram of an up/down counter, we can find _____

The next state of a given present state

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A Nibble consists of_____bits

4

The output of this circuit is always_____.

1

A logic circuit with an output X ABC AB consists of_____.

two AND gates, one OR gate, two inverters

The diagram given below represents _____

Sum of product form

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

DRAM stands for _____

Dynamic RAM

The three fundamental gates are _____

NOT, OR, AND

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Which of the following statement is true regarding above block diagram?

Triggering can take place anytime during the HIGH level of the CLK waveform

The expression F=A+B+C describes the operation of three bits_____Gate.

OR

Addition of two octal numbers “36” and “71” results in _____

127

The ANSI/IEEE Standard 754 defines a_____Single-Precision Floating Point format for binary numbers.

32-bit

The decimal “17” in BCD will be represented as _____

10111

The output of the expression F=A.B.C will be Logic_____when A=1, B=0, C=1.

Zero

_____is invalid number of cells in a single group formed by the adjacent cells in K-map

12

The PROM consists of a fixed non-programmable_____Gate array configured as a decoder.

AND

_____is one of the examples of asynchronous inputs. ?

J-K input

Consider an up/down counter that counts between 0 and 15, if external input(X) is “0” the countercounts upward (0000 to 1111) and if external input (X) is “1” the counter counts downward (1111 to0000), now suppose that the present state is “1100” and X=1, the next state of the counter will be_____.

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1101 (not sure)

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____is used to minimize the possible no. of states of a circuit.

State assignment

The best state assignment tends to_____.

Maximizes the number of state variables that don't change in a group of related states

5-bit Johnson counter sequences through_____states

10

The address from which the data is read, is provided by _____

Microprocessor

FIFO is an acronym for _____

First In, First Out

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

_____of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

Accuracy

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Above is the circuit diagram of_____.

Asynchronous up-counter

The sequence of states that are implemented by a n-bit Johnson counter is

2n (n multiplied by 2)

"A + B = B + A" is _____

Commutative Law

Following is standard POS expression

True

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

Using Iterative Circuit based Comparators

DE multiplexer is also called

Data distributor

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

_____Counters as the name indicates are not triggered simultaneously.

Asynchronous

In a state diagram, the transition from a current state to the next state is determined by

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Current state and the inputs

A synchronous decade counter will have_____flip-flops

4

The alternate solution for a demultiplexer-register combination circuit is

_____

Serial in / Parallel out shift register

The 4-bit 2"s complement representation of “+5” is _____

0101

The storage cell in SRAM is

a capacitor

What is the difference between a D latch and a D flip-flop?

The D flip-flop has a clock input.

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs

Will_____if the clock goes HIGH.

toggle

V OXFORD U BOOK SHOP

The OR gate performs Boolean_____.

addition

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

set

The power dissipation, PD, of a logic gate is the product of the

dc supply voltage and the peak current

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

True

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

True

Using multiplexer as parallel to serial converter requires_____connected to the multiplexer

A parallel to serial converter circuit

The 3-variable Karnaugh Map (K-Map) has_____cells for min or max terms

8

In designing any counter the transition from a current state to the next sate is determined by

Current state and inputs

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Sum term (Max term) is implemented using_____gates

OR

AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS “1”. WHAT WILL

BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

8 (not sure)

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

1

If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop

Invalid

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

J-K flip-flop

In_____Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop of the shift register.

Ring counter

The_____of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Access Time

Bi-stable devices remain in either of their_____states unless the inputs force the device to switch its state

Two

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

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8

A full-adder has a Cin = 0. What are the sum (<PRIVATE

"TYPE=PICT;ALT=sigma">) and the carry(Cout) when A = 1 and B = 1?

= 0, Cout = 1

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING

A _____

NEGATIVE-EDGE TRIGGERED FLIP-FLOPS

The design and implementation of synchronous counters start from _____

state diagram

THE HOURS COUNTER IS IMPLEMENTED USING _____

A SINGLE DECADE COUNTER AND A FLIP-FLOP

The high density FLASH memory cell is implemented using _____

1 floating-gate MOS transistor

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3

OXFORD BOOK SHOP

When the control line in tri-state buffer is high the buffer operates like a

_____gate

NOT

The output of an AND gate is one when _____

All of the inputs are one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

A > B = 1, A < B = 0, A = B = 0

The diagram above shows the general implementation of_____form

POS

The device shown here is most likely a

Multiplexer

DE multiplexer converts_____data to_____data

Serial data, parallel data

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

1

If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop

Invalid

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

A divide-by-50 counter divides the input_____signal to a 1 Hz signal.

OXFORD BOOK SHOP

50 Hz

The design and implementation of synchronous counters start from _____

state diagram

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called_____

In-System Programming (ISP)

Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.

XNOR

In_____outputs depend only on the combination of current state and inputs.

Mealy machine

In the following statement Z PIN 20 ISTYPE „reg.invert";

Active-low Registered Mode output

A Nibble consists of_____bits

4

A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing_____.

1001

OXFORD BOOK SHOP

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Fist In First Out Memory

If the FIFO Memory output is already filled with data then _____

None of given options

The process of converting the analogue signal into a digital representation (code) is known as_____

Quantization

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3

The simplest and most commonly used Decoders are the_____Decoders

n to 2n

In_____the output of the last flip-flop of the shift register is connected to the data input of the first flipflop. ?

Johnson counter

Which is not characteristic of a shift register?

Serial in/parallel in

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE

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The output of an XNOR gate is 1 when_____I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one

II and III only

NAND gate is formed by connecting _____

AND Gate and then NOT Gate

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

One

V OXFORD U BOOK SHOP

CS302 Quiz File

To write data to the memory the memory the write cycle is initiated by

Applying the address signals

The counter states or the range of the number of a counter is determined by the formula("n" represented

n

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the total number of flip-flops)

2 raise to power n

THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

OR

A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BYTHE MANUFACTURER.

TRUE

in sequential circuits memory elements are connected with_____.

common clock

A synchronous decade counter will have_____flip-flops

4

the terminal count of a modulus -13 binary counter is

1101

The alternate solution for a multiplexer and a register circuit is _____

Parallel in / Serial out shift register

A 8-bit serial in / parallel out shift register contains the value “8”,_____clock signal(s) will be required to shift the value completely out of the register.

8

Which of the following output equations determines the output of the state machine?

Max-Q0Q1EN

The CONSTATE.CLK = Clock is used to indicate that the_____state variables change on a clock transition.

CONSTATE

Memory is arranged in_____.

two-dimensional manner

The n flip-flops store_____states.

2^n

PALs tend to execute_____logic.

SOP

In DRAM read cycle R /W- signal is activated to read data which is made available on the_____data line.

D(OUT)

A SOP expression can be implemented by an _____ combination of gates.

AND-OR

Why demultiplexer is called a data distributor?

Single input to Single Output

If the number of samples that are collected is reduced

by half, the reconstructed signal will be _____ from/to the original.

Same

The AND Gate performs a logical_____function.

Division

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the_____can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The 64-cell array organized as 8 x 8 cell array is considered

as an 8 byte memory

A 3-variable karnaugh map has

eight cells

_____ Counters as the name indicates are not triggered simultaneously.

Synchronous

The ABEL Input file can use a_____instead of the equation to specify the Boolean expressions.

Truth Table

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The_____gate and_____gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

Flash memory Operation are classified into _____ different operation.

Two

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

The outputs of SR latches in elevator state machine are feed back to the_____gate array for connection to the D-flipflops.

AND

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The domain of the expression AB'CD + AB' + C'D + B is

A, B, C and D

The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.

1

Which of the following Output Equations determines

the output of the State Machine?

MAX = Q0Q1EN

When the transmission line is idle in an asynchronous transmission

It is set to logic high

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

NAND, NAND

PLDs have In-System Programming (ISP) capability that allows the_____to be programmed after they have been installed on a circuit board.

PLDs

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The terminal count of a 4-bit binary counter in the UP mode is_____.

1100

Select the mode of programming in which GAL16V8 can be programmed:

All of the given

Consider the sum of weight method for converting decimal into binary value,_____is the highest weight for 411.

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256

If two numbers in BCD representation generate an invalid BCD number then the binary_____is added to the result.

1001

In memory write cycle, the time for which the WE signal remains active is known as the_____.

Write pulse width

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a_____with a_____.

row, column

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

four

The Transition table is very similar to the _____ table.

State

A NOR based S-R latch is implemented using _____ gates instead of_____gates.

NOR, NAND

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using_____.

Shift Registers

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For a down counter that counts from (111 to 000), if current state is "101" the next state will be_____.

None of the given

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

NAND

The ROM used by a computer is relatively_____as it stores few byres of code used to Boot the Computer system on power up.

Small

Canonical form is a unique way of representing _____.

SOP

UVERPROM is stands for

Ultra-Voilet

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

1

Cin is part of_____Adder.

Full

Which one flip-flop has an invalid output state?

SR

Which of the following is a volatile memory?

DRAM

The maximum value, represented by a single hexadecimal digit is_____.

"F"

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack_____.

Top

8-bit parallel data can be converted into serial data by using_____multiplexer.

8-to-1

You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

NSY2 or EWY2

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

Adding two octal numbers "36" and "71" result in _____.

127

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store

a single bit of information.

High

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Demorgan's two theorems prove the equivalency of the NAND and_____gates and the NOR and _____ gates respectively.

Negative-OR, Negative-AND

A multiplexer with a register circuit converts

Parallel data to serial

Implementation of Latch is required almost _____ transistor.

Six

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as_____inputs.

Synchronous

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

Four

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be_____.

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One

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

4

The_____input overrides the_____input.

Asynchronous, synchronous

The Test Vector definition defines the test vectors for all the three counter inputs and_____counter output/outputs.

Three

Subtractors also have output to check if 1 has been _____.

Primed

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting_____.

Q output of all flip-flops to clock input of next flip-flops

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 32

For a Standard SOP expression, a_____is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Two signals_____and_____provide the timing inputs to the State Machine.

PTIME and QTIME

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

-WE

Implementation of the FIFO buffer in_____is usually takes the form of a circular buffer.

RAM

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in_____when Distributed refresh is used.

7.8 microsec

The output of a NAND gate is_____when all the inputs are one.

Zero

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------

THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

The terminal count of a 4-bit binary counter in the UP mode is .

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1111

For a down counter that counts from (111 to 000). If current state is “101” the next state will be

110

The n flip-flops store states.

2^n

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting

Q output of all flip-flops to clock input of next flip-flops

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated. Circuit counters allow cascading of multiple counters together.

True

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

False

The 74HC163 is a 4-bit Synchronous Counter, it has data output pins.

4

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 16

The synchronous counters are also known as Ripple Counters:

False

Each stage of Master-slave flip-flop works at of the clock signal

One half

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

80 micro seconds

Number of states in an 8-bit Johnson counter sequence are:

16

In moore machine the output depends on

The current state

Asynchronous mean that

Each flip-flop after the first one is enabled by the output of the preceding flip-flop

According to moore circuit, the output of synchronous sequential circuit depend/s on of flip flop.

Present state

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

0

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

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A one-shot mono-stable device contains _

NOR gate, Resistor, Capacitor and NOT Gate

The inputs can be directly mapped to karnaugh maps.

J-K

A mono-stable device only has a single stable state

True

When the Hz sampling interval is selected, the signal at the output of the J-K flipflop has a time period of seconds.

1, 2

The_____Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

1

NOR gate is formed by connecting _____

OR Gate and then NOT Gate

A particular half adder has

2 INPUTS AND 2 OUTPUT

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .

Toggle

A stage in the shift register consists of

A flip flop

If a circuit suffers “Clock Skew” problem, the output of circuit can’t be guarantied.

True

A modulus-14 counter has fourteen states requiring

4 flip flops

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

NOT

flip-flops are obsolete now.

Master-Slave

The glitches due to “Race Condition” can be avoided by using a .

Negative-Edge triggered flipflops

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=

1

occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock skew

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An Astable multivibrator is known as a (n) .

Oscillator

In Master-Slave flip-flop setup, the master flip-flop operators at

Both Master-Slave operator simultaneously

The power consumed by a flip-flop is defined by _

c.P = Vcc x Icc

The 3-bit up counter can be implemented using flip-flop(s).

S-R flip-flops and D-flip-flops

The terminal count of a 4-bit binary counter in the DOWN mode is

0000

If the S and R inputs of the gated S-R latch are connected together using a_____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

NOT

The low to high or high to low transition of the clock is considered to be a(n) _____

Edge

RCO Stands for _____

Ripple Clock Output

A transparent mode means _____

The changes in the data at the inputs of the latch are seen at the output

In_____outputs depend only on the current state.

Moore Machine

Smallest unit of binary data is a _____

Bit

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

State assignment

State of flip-flop can be switched by changing its

Input signal

Once the state diagram is drawn for any sequential circuit the next step is to draw

Next-state table

Design of state diagram is one of many steps used to design

A truncated counter

Flip flops are also called_____.

Bi-stable multivibrators

Three cascaded modulus-10 counters have an overall modulus of

1000

The term hold always means .

No change

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

J=X(Don't care),K=0

To parallel load a byte of data into a shift register, there must be

One clock pulse

Invalid state of NOR based SR latch occurs when _____.

S=1, R=1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called_____of the flip-flop.

Hold time

74HC163 has two enable input pins which are _____ and _____

ENP, ENT

_____ is said to occur when multiple internal variables change due to change in one input variable

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Race condition

The_____input overrides the _____ input

Asynchronous, synchronous

A decade counter is_____.

Mod-10 counter

In asynchronous transmission when the transmission line is idle, _____

It is set to logic high

A 8-bit serial in / parallel out shift register contains the value “8”,_____clock signal(s) will be required to shift the value completely out of the register.

8

In a sequential circuit the next state is determined by _____ and _____

Current state and external input

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

Mod-6, Mod-10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

True

A Nibble consists of_____bits

4

Excess-8 code assigns_____to “-8”

0000

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

LUT is acronym for _____

Look Up Table

The three fundamental gates are _____

NOT, OR, AND

The total amount of memory that is supported by any digital system depends upon _____

The size of the address bus of the microprocessor

Stack is an acronym for _____

LIFO memory

Addition of two octal numbers “36” and “71” results in _____

127

_____ is one of the examples of synchronous inputs.

J-K input

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

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Clock Skew

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____ is used to simplify the circuit that determines the next state.

State assignment

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

0000

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

Doesn't have an invalid state

A multiplexer with a register circuit converts _____

Parallel data to serial

GAL is essentially a_____.

Reprogrammable PAL

in_____, all the columns in the same row are either read or written.

FAST Mode Page Access

In order to synchronize two devices that consume and produce data at different rates, we can use _____

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Fist In First Out Memory

A flip-flop changes its state when _____

Low-to-high transition of clock

A frequency counter _____

Counts no. of clock pulses in 1 second

In a sequential circuit the next state is determined by _____ and _____

Input and clock signal applied

Flip flops are also called _____

Bi-stable multivibrators

Given the state diagram of an up/down counter, we can find _____

The next state of a given present state

A Nibble consists of_____bits

4

The output of this circuit is always_____.

1

A logic circuit with an output X ABC AB consists of _____.

two AND gates, one OR gate, two inverters

The diagram given below represents _____

Sum of product form

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The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

DRAM stands for _____

Dynamic RAM

The three fundamental gates are _____

NOT, OR, AND

Which of the following statement is true regarding above block diagram?

Triggering can take place anytime during the HIGH level of the CLK waveform

The expression F=A+B+C describes the operation of three bits_____Gate.

OR

Addition of two octal numbers “36” and “71” results in _____

127

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The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

32-bit

The decimal “17” in BCD will be represented as _____

10111

The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

Zero

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

12

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

AND

_____ is one of the examples of asynchronous inputs. ?

J-K input

Consider an up/down counter that counts between 0 and 15, if external input(X) is “0” the countercounts upward (0000 to 1111) and if external input (X) is “1” the counter counts downward (1111 to0000), now suppose that the present state is “1100” and X=1, the next state of the counter will be_____.

1101 (not sure)

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____ is used to minimize the possible no. of states of a circuit.

State assignment

The best state assignment tends to_____.

Maximizes the number of state variables that don't change in a group of related states

5-bit Johnson counter sequences through_____states

10

The address from which the data is read, is provided by _____

Microprocessor

FIFO is an acronym for _____

First In, First Out

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

Accuracy

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Above is the circuit diagram of_____.

Asynchronous up-counter

The sequence of states that are implemented by a n-bit Johnson counter is

2n (n multiplied by 2)

"A + B = B + A" is _____

Commutative Law

Following is standard POS expression

True

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

Using Iterative Circuit based Comparators

DE multiplexer is also called

Data distributor

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

_____ Counters as the name indicates are not triggered simultaneously.

Asynchronous

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

A synchronous decade counter will have_____flip-flops

4

The alternate solution for a demultiplexer-register combination circuit is _____

Serial in / Parallel out shift register

The 4-bit 2"s complement representation of “+5” is _____

0101

The storage cell in SRAM is

a capacitor

What is the difference between a D latch and a D flip-flop?

The D flip-flop has a clock input.

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs Will_____if the clock goes HIGH.

toggle

The OR gate performs Boolean_____.

addition

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

set

The power dissipation, PD, of a logic gate is the product of the

dc supply voltage and the peak current

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

True

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NOR Gate can be used to perform the operation of AND, OR and NOT Gate

True

Using multiplexer as parallel to serial converter requires_____connected to the multiplexer

A parallel to serial converter circuit

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

8

In designing any counter the transition from a current state to the next sate is determined by

Current state and inputs

Sum term (Max term) is implemented using _____ gates

OR

AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL

BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

8 (not sure)

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

1

If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop

Invalid

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

J-K flip-flop

In_____Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop of the shift register.

Ring counter

The_____of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Access Time

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

Two

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8

A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry(Cout) when A = 1 and B = 1?

= 0, Cout = 1

THE GLITCHES DUE TO RACE CONDITION CAN

BE AVOIDED BY USING A _____

NEGATIVE-EDGE TRIGGERED FLIP-FLOPS

The design and implementation of synchronous counters start from _____

state diagram

THE HOURS COUNTER IS IMPLEMENTED USING _____

A SINGLE DECADE COUNTER AND A FLIP-FLOP

The high density FLASH memory cell is implemented using _____

1 floating-gate MOS transistor

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3

When the control line in tri-state buffer is high the buffer operates like a_____gate

NOT

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The output of an AND gate is one when _____

All of the inputs are one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

A > B = 1, A < B = 0, A = B = 0

The diagram above shows the general implementation

of_____form

POS

The device shown here is most likely a

Multiplexer

DE multiplexer converts_____data to _____data

Serial data, parallel data

If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop

1

If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop

Invalid

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

A divide-by-50 counter divides the input_____signal to a 1 Hz signal.

50 Hz

The design and implementation of synchronous

counters start from _____

state diagram

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called_____

In-System Programming (ISP)

Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.

XNOR

In_____outputs depend only on the combination of current state and inputs.

Mealy machine

In the following statement Z PIN 20 ISTYPE „reg.invert";

Active-low Registered Mode output

A Nibble consists of_____bits

4

A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing_____.

1001

In order to synchronize two devices that consume and produce data at different rates, we can use _____

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Fist In First Out Memory

If the FIFO Memory output is already filled with data then _____

None of given options

The process of converting the analogue signal into a digital representation (code) is known as _____

Quantization

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3

The simplest and most commonly used Decoders are the_____Decoders

n to 2n

In_____the output of the last flip-flop of the shift register is connected to the data input of the first flipflop. ?

Johnson counter

Which is not characteristic of a shift register?

Serial in/parallel in

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE

The output of an XNOR gate is 1 when _____
I) All the inputs are zero II) Any of the inputs is zero
III) Any of the inputs is one IV) All the inputs are one

II and III only

NAND gate is formed by connecting _____

AND Gate and then NOT Gate

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

One

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ANYWHERE ANYTIME

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Question No: 1
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
► Set-up time
► **Hold time (Page 242)**
► Pulse Interval time
► Pulse Stability time (PST)

Question No: 2
74HC163 has two enable input pins which are_____and _____
► **ENP, ENT (Page 285)**
► ENI, ENC
► ENP, ENC
► ENT, ENI

Question No: 3
_____is said to occur when multiple internal variables change due to change in one input variable
► Clock Skew
► **Race condition (Page 267)**
► Hold delay
► Hold and Wait

Question No: 4
The_____input overrides the_____input
► **Asynchronous, synchronous (Page 369)**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 5
A decade counter is_____.
► Mod-3 counter
► Mod-5 counter
► Mod-8 counter
► **Mod-10 counter (Page 274)**

Question No: 6
In asynchronous transmission when the transmission line is idle, _____
► It is set to logic low
► **It is set to logic high (Page 356)**
► Remains in previous state
► State of transmission line is not used to start transmission

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Question No: 7 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8",_____clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356)**

Question No: 8

In a sequential circuit the next state is determined by_____and _____

► State variable, current state
► Current state, flip-flop output
► **Current state and external input (Page 318)**
► Input and clock signal applied

Question No: 9

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 299)**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

Question No: 10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► **True (Page 221)**
► False

Question No: 11

A Nibble consists of_____bits

► 2
► **4 (Page 394)**
► 8
► 16

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Question No: 12

Excess-8 code assigns_____to "-8"

► 1110
► 1100
► 1000
► **0000 (Page 34)**

Question No: 13

The voltage gain of the Inverting Amplifier is given by the relation _____

► **Vout / Vin = - Rf / Ri (Page 446)**
► Vout / Rf = - Vin / Ri
► Rf / Vin = - Ri / Vout
► Rf / Vin = Ri / Vout

Question No: 14
LUT is acronym for _____
► **Look Up Table (Page 439)**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 15
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page 40)**

Question No: 16
The total amount of memory that is supported by any digital system depends upon _____
► The organization of memory
► The structure of memory
► The size of decoding unit
► **The size of the address bus of the microprocessor (Page 430)**

Question No: 17
Stack is an acronym for _____
► FIFO memory
► **LIFO memory (Page 429)**
► Flash Memory
► Bust Flash Memory

Question No: 18
Addition of two octal numbers "36" and "71" results in _____
► 213
► 123
► **127**
► 345

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Question No: 19
_____is one of the examples of synchronous inputs.
► **J-K input (Page 235)**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 20
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
► Race condition
► **Clock Skew (Page 226)**

► Ripple Effect
► None of given options

Question No: 22
In a state diagram, the transition from a current state to the next state is determined by
► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 23
_____is used to simplify the circuit that determines the next state.
► State diagram
► Next state table
► State reduction
► **State assignment (Page 335)**

Question No: 24
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)
► 1100
► 0011
► 0000
► 1111

Question No: 25
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____.
► **Doesn't have an invalid state (Page 232)**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 26
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356)**
► Serial data to serial
► Parallel data to parallel

Question No: 27
GAL is essentially a_____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183)**

Question No: 28
in_____, all the columns in the same row are either read or written.
► Sequential Access
► MOS Access
► **FAST Mode Page Access (Page 413)**
► None of given options

Question No: 29
In order to synchronize two devices that consume and produce data at different rates, we can use _____
► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 30
A flip-flop changes its state when _____
► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 31
A frequency counter _____
► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301)**
► Counts high and low range of given clock pulse
► None of given options

Question No: 32
In a sequential circuit the next state is determined by_____and _____
► State variable, current state
► Current state, flip-flop output
► Current state and external input
► **Input and clock signal applied (Page 305)**

Question No: 33
Flip flops are also called _____
► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

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Question No: 36

Given the state diagram of an up/down counter, we can find _____

► **The next state of a given present state (Page 371)**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

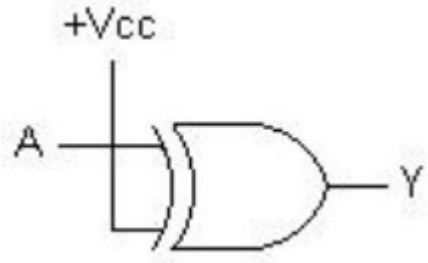
Question No: 38

A Nibble consists of_____bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 39

The output of this circuit is always_____.



► 1
► 0
► A
► $\overline{A}$

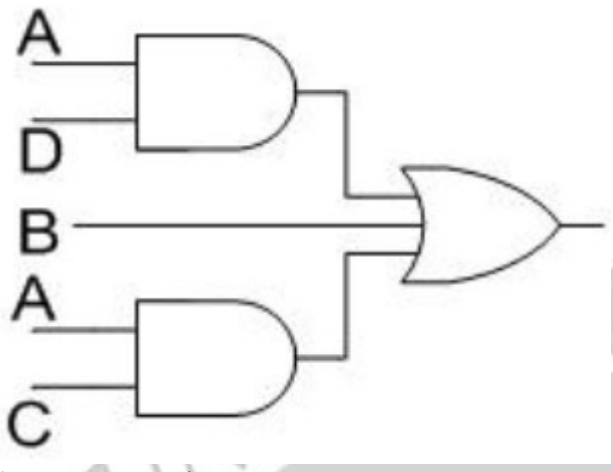
Question No: 40

A logic circuit with an output $X = ABC + \overline{A}\overline{B}$ consists of_____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► **two AND gates, one OR gate, two inverters (Lecture 8)**
► two AND gates, one OR gate

Question No: 41

The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78)**

Question No: 42
The voltage gain of the Inverting Amplifier is given by the relation _____
► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

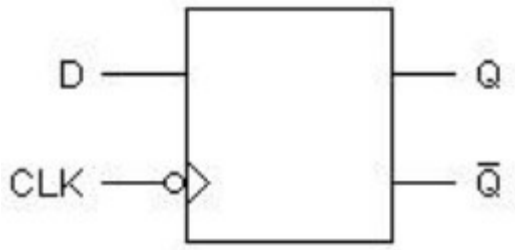
Question No: 43
DRAM stands for _____
► **Dynamic RAM (Page 407)**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 44
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page**

40) Question No: 45

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Which of the following statement is true regarding above block diagram?
► Triggering takes place on the negative-going edge of the CLK pulse
► Triggering takes place on the positive-going edge of the CLK pulse
► Triggering can take place anytime during the HIGH level of the CLK waveform
► Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 46
The expression F=A+B+C describes the operation of three bits_____Gate.
► **OR (Page 42)**
► AND
► NOT
► NAND

Question No: 47
Addition of two octal numbers "36" and "71" results in _____
► 213
► 123
► **127**
► 345

Question No: 48
The ANSI/IEEE Standard 754 defines a_____Single-Precision Floating Point format for binary numbers.
► 8-bit
► 16-bit
► **32-bit (Page 25)**
► 64-bit

Question No: 49
The decimal "17" in BCD will be represented as _____
► 11101
► 11011
► **10111 (According to rule)**
► 11110

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Question No: 50
The basic building block for a logical circuit is _____
► A Flip-Flop
► **A Logical Gate (Page 7)**
► An Adder
► None of given options

Question No: 51
The output of the expression F=A.B.C will be Logic_____when A=1, B=0, C=1.
► Undefined
► One
► **Zero (According to rule)**
► No Output as input is invalid.

Question No: 52
_____is invalid number of cells in a single group formed by the adjacent cells in K-map
► 2
► 8
► **12 (According to rule "2^n")**
► 16

Question No: 53
The PROM consists of a fixed non-programmable_____Gate array configured as a decoder.
► **AND (Page 182)**
► OR
► NOT
► XOR

Question No: 54
_____is one of the examples of asynchronous inputs. ► J-K input
► S-R input
► D input

► **Clear Input (CLR) (Page 235)** **Question No: 55**
Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be

_____
► 0000
► **1101 (not sure)**
► 1011
► 1111

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Question No: 56

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 232)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 57

_____is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341)**
► State reduction
► Next state table
► State diagram

Question No: 59

The best state assignment tends to_____.

► **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
► Minimizes the number of state variables that don't change in a group of related states
► Minimize the equivalent states
► None of given options

Question No: 60

5-bit Johnson counter sequences through_____states

► 7
► **10 (Page 354)**
► 32
► 25

Question No: 61

The address from which the data is read, is provided by _____

► Depends on circuitry
► None of given options
► RAM
► **Microprocessor (Page 397)**

Question No: 62

FIFO is an acronym for _____

► **First In, First Out (Page 424)**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 63

The voltage gain of the Inverting Amplifier is given by the relation _____

► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**

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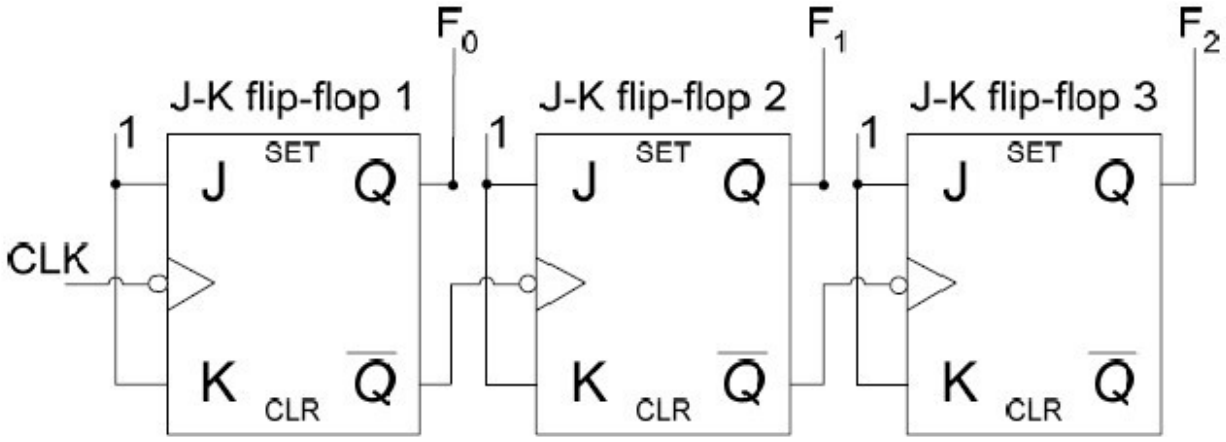
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 64

_____of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

► Resolution
► **Accuracy (Page 460)**
► Quantization
► Missing Code

Question No: 65



Above is the circuit diagram of_____.

► **Asynchronous up-counter (Page 270)**
► Asynchronous down-counter
► Synchronous up-counter
► Synchronous down-counter

Question No: 66

The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354)**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

Question No: 67

"A + B = B + A" is _____

► Demorgan"s Law
► Distributive Law
► **Commutative Law (Page 72)**
► Associative Law

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Question No: 68

Following is standard POS expression

$$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$$

► **True (Lecture 9)**
► False

Question No: 69

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

► Using a single comparator
► **Using Iterative Circuit based Comparators (Page 155)**
► Connecting comparators in vertical hierarchy
► Extra logic gates are always required.

Question No: 70

DE multiplexer is also called

► Data selector
► Data router
► **Data distributor (Page 178)**
► Data encoder

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Question No: 71

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 72

_____Counters as the name indicates are not triggered simultaneously.

► **Asynchronous (Page 269)**
► Synchronous
► Positive-Edge triggered
► Negative-Edge triggered

Question No: 74
In a state diagram, the transition from a current state to the next state is determined by
► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 75
A synchronous decade counter will have_____flip-flops
► 3
► **4 (Page 281)**
► 7
► 10

Question No: 76
The alternate solution for a demultiplexer-register combination circuit is _____
► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356)**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 77
The 4-bit 2"s complement representation of "+5" is _____
► 1010
► 1110
► 1011
► **0101 (Page 22)**

Question No: 78
The storage cell in SRAM is
► a flip –flop
► **a capacitor (Page 407)**
► a fuse
► a magnetic domain

Question No: 79
What is the difference between a D latch and a D flip-flop?
► The D latch has a clock input.
► The D flip-flop has an enable input.
► The D latch is used for faster operation.
► **The D flip-flop has a clock input.**

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Question No: 80

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs Will if the clock goes HIGH.

► **toggle**
► set
► reset
► not change

Question No: 81

The OR gate performs Boolean_____.

► multiplication
► subtraction
► division
► **addition (Page 42)**

Question No: 82

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

► **set (Page 219)**
► reset
► invalid
► clear

Question No: 83

Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.

► A = 1, B = 0, C = 0, D = 0
► **A = 1, B = 0, C = 1, D = 0 (Lecture 8)**
► A = 0, B = 1, C = 0, D = 0
► A = 1, B = 0, C = 1, D = 1

Question No: 84

The power dissipation, *P*D, of a logic gate is the product of the

► **dc supply voltage and the peak current**
► dc supply voltage and the average supply current
► ac supply voltage and the peak current
► ac supply voltage and the average supply current

Question No: 85

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True**
► False

Question No:86

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **True (Page 50)**
► False

Question No: 87

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Using multiplexer as parallel to serial converter requires_____connected to the multiplexer
► A parallel to serial converter circuit (Page 244)
► A counter circuit
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

Question No: 88
The 3-variable Karnaugh Map (K-Map) has_____cells for min or max terms
►4
► 8 (Page 89)
►12
►16

Question No: 89
In designing any counter the transition from a current state to the next sate is determined by
► Current state and inputs (Page 332)
► Only inputs
► Only current state
► current state and outputs

Question No: 90
Sum term (Max term) is implemented using_____gates
► OR (Page 78)
► AND
► NOT
► OR-AND

Question No: 91
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?
►2
►4
►6
► 8 (not sure)

Question No: 93
If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop
►0
► 1 (Page 230)
► Invalid
► Input is invalid

Question No: 94
If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop
► 0
► 1
► Invalid (Page 233)

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► Input is invalid

Question No: 95

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

►Using S-R Flop-Flop
►D-flipflop
►J-K flip-flop (Page 252)
►T-Flip-Flop

Question No: 96

A counter is implemented using three (3) flip-flops, possibly it will have_____maximum output status.

►3
►7
►8 (Page 272)
►15

Question No: 97

In_____Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

►Moore machine
►Mealy machine
►Johnson counter
►Ring counter (Page 355)

Question No: 98

The_____of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

►Write Time
►Recycle Time
►Refresh Time
►Access Time (Page 417)

Question No: 99

Bi-stable devices remain in either of their_____states unless the inputs force the device to switch its state

►Ten
►Eight
►Three
►Two (Page 262)

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Question No: 101

A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

►= 0, Cout = 0

►= 0, Cout = 1 (Page 135)

►= 1, Cout = 0

►= 1, Cout = 1

Question No: 102

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

► GATED FLIP-FLOPS

► PULSE TRIGGERED FLIP-FLOPS

► POSITIVE-EDGE TRIGGERED FLIP-FLOPS

► NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)

Question No: 103

The design and implementation of synchronous counters start from _____

► Truth table

► k-map

► state table

► state diagram (Page 319)

Question No: 104

THE HOURS COUNTER IS IMPLEMENTED USING _____

► ONLY A SINGLE MOD-12 COUNTER IS REQUIRED

► MOD-10 AND MOD-6 COUNTERS

► MOD-10 AND MOD-2 COUNTERS

► A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)

Question No: 105 (Marks: 1) - Please choose one

The high density FLASH memory cell is implemented using _____

► 1 floating-gate MOS transistor (Page 419)

► 2 floating-gate MOS transistors

► 4 floating-gate MOS transistors

► 6 floating-gate MOS transistors

Question No: 106 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

► Q2:= Q1 $ X $ Q3

► Q2:= Q1 # X # Q3 (Page 210)

► Q2:= Q1 & X & Q3

► Q2:= Q1 ! X ! Q3

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Question No: 107

Generally, the Power dissipation of_____devices remains constant throughout their operation.

► TTL (Page 65)

► CMOS 3.5 series

► CMOS 5 Series

► Power dissipation of all circuits increases with time.

Question No: 108

When the control line in tri-state buffer is high the buffer operates like a_____gate

► AND

► OR

► NOT (Page 196)

► XOR

Question No: 109

v CMOS series is characterized by_____and_____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation

► Fast switching speeds, high power dissipation

► Fast switching speeds, very low power dissipation (Page 61)

► Low switching speeds, very low power dissipation

Question No:110

The output of an AND gate is one when _____

► All of the inputs are one (Page 40)

► Any of the input is one

► Any of the input is zero

► All the inputs are zero

Question No: 111

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1

► A > B = 0, A < B = 1, A = B = 0

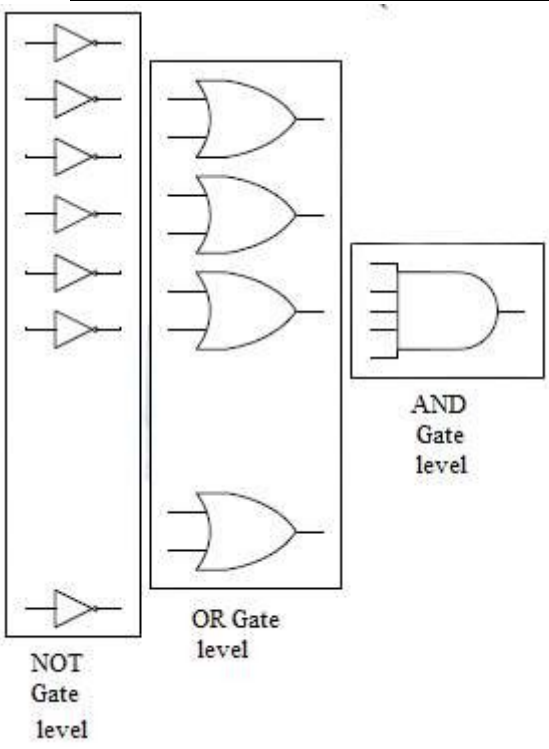
► A > B = 1, A < B = 0, A = B = 0 (Page 109)

► A > B = 0, A < B = 1, A = B = 1

Question No:112

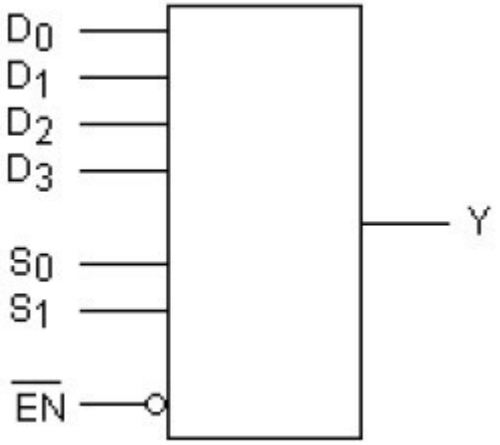
The diagram above shows the general implementation of_____form

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- boolean
- arbitrary
- **POS (Page 122)**
- SOP

Question No: 113
The device shown here is most likely a



- Comparator
- Multiplexer
- Demultiplexer
- Parity generator

Question No: 114

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DE multiplexer converts_____data to_____
data
► Parallel data, serial data
► **Serial data, parallel data (Page 356)**
► Encoded data, decoded data
► All of the given options.

Question No:115
If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop
► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 116
If S=1 and R=1, then Q(t+1) =_____for negative edge triggered flip-flop
► 0
► 1
► **Invalid (Page 230)**
► Input is invalid

Question No: 119
In asynchronous digital systems all the circuits change their state with respect to a common clock
► True
► **False (Page 245)**

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Question No: 201
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is
► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 202
A divide-by-50 counter divides the input_____signal to a 1 Hz signal.
► 10 Hz
► **50 Hz (Page 298)**
► 100 Hz
► 500 Hz

Question No: 203
The design and implementation of synchronous counters start from _____
► Truth table
► k-map
► state table
► **state diagram (Page 319)**

Question No: 204
In_____the output of the last flip-flop of the shift register is connected to the data input of the first flip-flop. ► Moore machine
► Mealy machine
► **Johnson counter (Page 354)**
► Ring counter Q

Question No: 205
Which is not characteristic of a shift register?
► **Serial in/parallel in (Page 346)**
► Serial in/parallel out
► Parallel in/serial out
► Parallel in/parallel out

Question No:206
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
► FALSE
► **TRUE (Page 250)**

Question No: 207
The output of an XNOR gate is 1 when_____I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one
► I Only
► IV Only
► I and IV only
► **II and III only (Page 53)**

Question No: 208
NAND gate is formed by connecting _____
► **AND Gate and then NOT Gate (Page 45)**
► NOT Gate and then AND Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

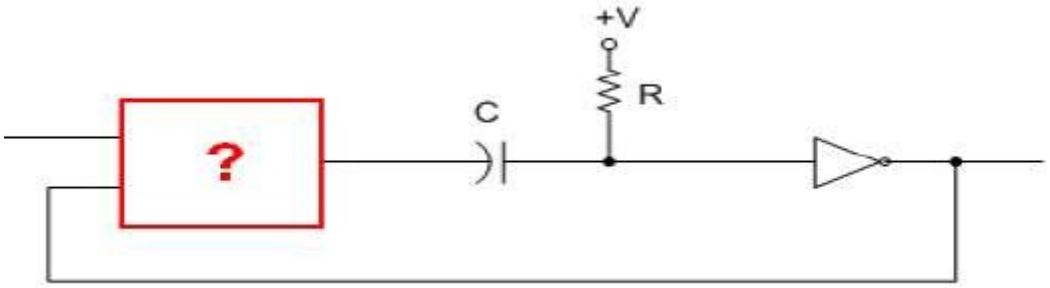
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Question No: 209
Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____
► Zero
► **One (Page 46)**
► Undefined
► No output as input is invalid

Question No: 210
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____
► Radiation-Erase programming method (REPM)
► **In-System Programming (ISP) (Page 194)**
► In-chip Programming (ICP)
► Electronically-Erase programming method(EEPM)

Question No: 211
Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.



► AND
► NAND
► NOR
► **XNOR (Page 262)**

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Question No: 212
In_____outputs depend only on the combination of current state and inputs.
► **Mealy machine (Page 332)**
► Moore Machine
► State Reduction table
► State Assignment table

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Question No: 213
In the following statement Z PIN 20 ISTYPE „reg.invert“;
The keyword “reg.invert” indicates _____
► An inverted register input
► An inverted register input at pin 20
► Active-high Registered Mode output
► **Active-low Registered Mode output (Page 360)**

Question No: 214
A Nibble consists of_____bits
► 2
► **4 (Page 394)**
► 8
► 16

Question No: 215
A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing_____.
► 1110
► 0111
► 1000
► **1001**

Question No: 216
In order to synchronize two devices that consume and produce data at different rates, we can use _____
► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 217
If the FIFO Memory output is already filled with data then _____
► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 218
The process of converting the analogue signal into a digital representation (code) is known as _____
► Strobing
► Amplification
► **Quantization (Page 445)**
► Digitization

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Question No: 219

$(A \cdot B)(A \cdot \overline{B} \cdot C)(\overline{A} \cdot C)$
is an example of _____

► **Product of sum form (Page 77)**
► Sum of product form
► Demorgans law
► Associative law

Question No: 220

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be
► Q2:= Q1 $ X $ Q3
► **Q2:= Q1 # X # Q3 (Page 210)**
► Q2:= Q1 & X & Q3
► Q2:= Q1 ! X ! Q3

Question No: 221

Caveman number system is Base_____number system ► 2
► **5 (Page 11)**
► 10
► 16

Question No: 222

The output of an XOR gate is zero (0) when _____
I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 223

The simplest and most commonly used Decoders are the_____Decoders
► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

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Question No: 224
The_____Encoder is used as a keypad encoder.
► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► **Decimal-to-BCD Priority (Page 166)**

Question No: 225
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions
► **True (Page 161)**
► False

Question No: 226
If S=1 and R=0, then Q(t+1) =_____for positive edge triggered flip-flop
► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 227
If the S and R inputs of the gated S-R latch are connected together using a_____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)
► AND
► OR
► **NOT (Page 226)**
► XOR

Question No: 228
The low to high or high to low transition of the clock is considered to be a(n) _____
► State
► **Edge (Page 228)**
► Trigger
► One-shot

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Question No: 230
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► **Ripple Clock Output (Page 285)**

Question No: 231
A transparent mode means _____
► **The changes in the data at the inputs of the latch are seen at the output (Page 245)**
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

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Question No: 232
In_____outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 233
Smallest unit of binary data is a _____
► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 234
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 235
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 236
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT_____GATE
► AND
► **OR (Page 171)**
► NAND
► XOR

Question No: 237
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.
► **TRUE (Page 182)**
► FALSE

Question No: 241
A synchronous decade counter will have_____flip-flops
► 3
► **4 (Page 281)**
► 7

► 10

Question No: 242

The alternate solution for a multiplexer and a register circuit is _____

► **Parallel in / Serial out shift register (Page 356)**

► Serial in / Parallel out shift register

► Parallel in / Parallel out shift register

► Serial in / Serial Out shift register

Question No: 243

A 8-bit serial in / parallel out shift register contains the value "8",_____clock signal(s) will be required to shift the value completely out of the register.

► 1

► 2

► 4

► **8 (Page 356)**

Question No: 245

If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter

► It is not locked; the new data overwrites the previous data.

► Previous data is swapped out of memory and new data enters

► **None of given options**

Question No: 246

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO ------

► THE FLOP-FLOP IS TRIGGERED

► Q=0 AND Q‟=1

► Q=1 AND Q‟=0

► **THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)**

Question No: 247

The terminal count of a 4-bit binary counter in the UPmode is____.

- 1100
- 0011
- 1111
- 0000

Question No: 248

For a down counter that counts from (111 to 000). If current state is "101" the next state willbe ____.

- 111
- 110
- 010
- None of given options

Question No: 249

The n flip-flops store_____states.

a. 1

b.

2^n

c. 0

d. 2^(n+1)

Question No: 250

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting _____.

- Q output of all flip-flops to clock input of next flip-flops
- Q' output of all flip-flops to clock input of next flip-flops
- Q output of all flip-flops to J input of next flip-flops
- Q' output of all flip-flops to K input of next flip-flops

Question No: 251

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together.

- True
- False

Question No: 251

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

a.True

b.False

Question No: 252

The 74HC163 is a 4-bit Synchronous Counter, it has_____data output pins.

b. 2

b. 4

c. 6

d. 8

Question No: 253

Divide-by-32 counter can be achieved by using

c. Flip-Flop and DIV10b. Flip-Flop and DIV 16

c. Flip-Flop and DIV 32

d. DIV 16 and DIV 32

Question No: 254

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The synchronous counters are also known as Ripple Counters:

a.True

b False

Question No: 255

Each stage of Master-slave flip-flop works at_____of the clock signal

- Each stage works on complete clock signal
- One fourth
- One third
- One half

Question No: 256

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

`

a. 80 micro seconds

b. 8 micro seconds

c. 80 mili seconds

d. 10 micro seconds

Question No: 257

Number of states in an 8-bit Johnson counter sequence are:

d. 8

e. 12

f. 14

g. 16

Question No: 258

In moore machine the output depends on

- The current state and the output of previous flip flop
- Only inputs
- The current state
- The current state and inputs

Question No: 259

Asynchronous mean that _____

- Each flip-flop after the first one is enabled by the output of thepreceding flip-flop
- Each flip-flop is enabled by the output of the preceding flip-flop
- Each flip-flop except the last one is enabled by the output of the preceding flip-flop
- Each alternative flip-flop after the first one is enabled by the output of the precedingflip-flop

Question No: 260

According to moore circuit, the output of synchronous sequential circuit depend/s on _____of flip flop.

h. Previous state

i. Present state

j. Next state

k. External state

Question No: 261

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

- Q
- 0

- 1
- Invalid

Question No: 262

A Divide-by-20 counter can be achieved by using

a. Flip-Flop and DIV 10
b. Flip-Flop and DIV 16
c. Flip-Flop and DIV 32
d. DIV 10 and DIV 16

Question No: 263

A one-shot mono-stable device contains_____

- AND gate, Resistor, Capacitor and NOT Gate
- NAND gate, Resistor, Capacitor and NOT Gate
- NOR gate, Resistor, Capacitor and NOT Gate

- XNOR gate, Resistor, Capacitor and NOT Gate

Question No: 264

The inputs can be directly mapped to karnaugh maps.

- S-R
- J-K
- Flip-Flop
- External

Question No: 265

A mono-stable device only has a single stable state

a. True
b. False

Question No: 266

When the_____Hz sampling interval is selected, the signal at the output of the J-K flip-flophas a time period of_____seconds.

a. 1, 2
b. 0, 2
c. 2, 5
d. 1, 1

Question No: 267

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to_____.

- Set
- Toggle

- Latch
- Reset

Question No: 268

A stage in the shift register consists of

- A latch
- A flip flop
- A byte of storage
- Four bits of storage

Question No: 269

If a circuit suffers "Clock Skew" problem, the output of circuit can't be guarantied.

a. True

b. False

Question No: 270

A modulus-14 counter has fourteen states requiring _____

l. 14 flip flops

m. 14 registers

c. 4 flip flops

d. 4 registers

Question No: 271

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using_____gate.

- AND
- OR
- NOT
- NAND

Question No: 272

_____flip-flops are obsolete now.

- Edge-triggered
- Master-Slave
- T-flipflop
- D-flipflop

Question No: 273

The glitches due to "Race Condition" can be avoided by using a_____.

n. Gated flip-flops

o. Pulse triggered flip-flops

p. Positive-Edge triggered flip-flops

d. Negative-Edge triggered flip-flops

Question No: 274

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=_____

- 0
- Q(t)

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- 1
- Invalid

Question No: 275

____occurs when the same clock signal arrives at different times at different clockinputs due to propagation delay.

q. Race condition
b. Clock skew
c. Ripple effect
d. None of given options

Question No: 276

An Astable multivibrator is known as a (n)_____.

a. Oscillator
b. Booster
c. One-shot
d. Dual-shot

Question No: 277

In Master-Slave flip-flop setup, the master flip-flop operators at _____

- Positive half cycle of pulse
- Negative half cycle of pulse
- Both Master-Slave operator simultaneously
- Master-Slave flip-flop does not operate on pulses rather it is edge triggered

Question No: 278

The power consumed by a flip-flop is defined by _____

- P = Icc x Rcc
- P=vcc x Rcc
- c.P = Vcc x Icc
- P = Mcc x Vcc

Question No: 279

The 3-bit up counter can be implemented using_____flip-flop(s).

- S-R flip-flops only
- S-R flip-flops and D-flip-flops
- S-R flip-flops or D-flip-flops
- D-flip-flop only

Question No: 280

The terminal count of a 4-bit binary counter in the DOWN mode is _____

a. 0000
b. 0011
c. 1100
d. 1111

Question No: 281

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

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- State reduction
- State minimization

State assignment

- State evaluation

Question No: 282

State of flip-flop can be switched by changing its _____

a. Input signal
b. Output signal
c. Momentary signal
d. Contemporary signal

Question No: 283

Once the state diagram is drawn for any sequential circuit the next step is to draw

- Transiation table
- Karnaugh map
- Next-state table
- Logic expression

Question No: 284

Design of state diagram is one of many steps used to design

- A clock
- A truncated counter
- An UP/DOWN counter
- Any counter

Question No: 285

Flip flops are also called _____

- Bi-stable multivibrators
- Bi-stable singlevibrators
- Bi-stable dualvibrators
- Bi-stable transformer

Question No: 286

Three cascaded modulus-10 counters have an overall modulus of

- 30
- b. 100
- c. 1000

10000

Question No: 287

The term hold always means_____.

a. Q=0, Q'=1
b. Q=1, Q'=0
c. Q=0, Q'=0
d. No change

Question No: 288

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

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a. J=1, K=0
b. J=1,K=X(Don'tcare)
c. J=X(Don'tcare),K=0
d. J=0, K=X(Don't care)

Question No: 289

To parallel load a byte of data into a shift register, there must be

a. One clock pulse
b. One clock pulse for each 1 in the data
c. Eight clock pulse
d. One clock pulse for each 0 in the data

Question No: 290

Invalid state of NOR based SR latch occurs when_____.

r. S=0, R=0
s. S=0, R=1
t. S=1, R=0
u. S=1, R=1

1. The transition table is very similar to the_____table
   a. Truth
   b. State page 382
   c. Transition
   d. None of the given option

2. Two Signals_____and_____provide the timing inputs to the state machine
   a. NSSR and EWSR
   b. LTIME and STIME page 374
   c. PTIME and QTIME
   d. NSGrn and NSYel
3. Memories are implemented in_____bit data unit sizes
   a. 1 , 2 and 6
   b. 2 , 3 and 6
   c. 1 , 4 and 8 page 425
   d. 4 , 5 and 8
4. In distributed mode, for a 1024 X 1024 DRAM memory and a refresh cycle of 8msec, each of the 1024 rows has to be refreshed in_____when distributed refresh is used
   a. 4.8 microsec
   b. 5.9 micorsec
   c. 7.8 micorsec page 406

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d. 5.5 microsec

5. The EPROM uses_____array with an isolated gate structure
   a. NMOSFET page 411
   b. MOSFETK
   c. UVMOSFT
   d. None of the given options
6. The 64-cell array organized as 8 X 8 cell array is considered
   a. As an 64 byte memory
   b. As a 16 byte memory
   c. As an 8 byte memory page 387
   d. As an 4 byte memory
7. The test vector definition defines the test vector for all the three counter inputsand___counter output/outputs
   a. One
   b. Two
   c. Three page 362
   d. Four
8. In memory write cycle, the time for which the WE signal remains active isknown as the _____
   a. Write address setup
   b. Write pulse width page 397
   c. Write delay width
   d. Write DataTime

9. If the voltage drop across the active load is 0 volts due to absence of current thecomparator output is a_____
   a. 0
   b. 1 page 417
10. As data values are written or read from RAM stack, the stack pointer registerincrements or decrements its contents always pointing to the stack

    a. Bottom
    b. Top page 422
    c. Down
    d. Vertex
11. A 4-bit binary up/down counter in in the binary state of zero. The next state inthe DOWN mode is?
    a. 0001
    b. 1000

c. 1110
d. 1111

12. Flash memory operation are classified into_____different operations
    a. Two
    b. Three page 413
    c. Four
    d. Five
13. Implementation of latch is required almost_____transistor?
    a. Two
    b. Four
    c. Six page 417
    d. Eight
14. In elevator circuit, the floor display circuit is a combinational circuit which uses the_____and_____inputs two determine the floor number and the function of the display arrow.
    a. CONSTATE, FB
    b. OPEN, DIR
    c. MOTION, DIR page 374
    d. MOTION, FB

15. The bit capacity of memory that has 1024 addresses and can store 8 bit at each address is
    a. 8
    b. 1024
    c. 4096
    d. 8192 page 388(memory capacity) 1024*8=8192
16. When the transmission line is idle in an asynchronous transmission
    a. It is set to logic low
    b. It set to logic high page 349
    c. It remains in previous state
    d. State of transmission line is not used to start transmission17.Which of the following is a volatile memory?
    a. PROM
    b. DRAM page 400(capacitor based ROM, need extra circuit to retain the memory)
    c. EPROM
    d. EEPROM
18. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration t_{WD} ?

a. `CS
b. `WE page 397
c. W
d. OE

19. The ROM used by computer is relatively very_____asitstores fewbytes of code used to boot the computer system on power up
a. Small page 423
b. Large
c. Heavy
d. High

20. In DRAM read cycle R/W signal is activated to read data which is madeavailableonthe____Data line
a. D(IN)
b. D(OUT) page 405
c. D(AB)
d. D(INT)

21. _____Yellow signal controlling the traffic on the east–westsection.
a. NSGrn
b. NSYel
c. EWYel page 375
d. EWRed

22. A 32 bit data word consists of :
a. 2 bytes
b. 4 Bytes page 387
c. 2 nibbles
d. 4 nibbles

complete unit of information is sometimes called a _____
a. Bit
b. Nibble
c. Word(correct) page 387
d. Byte

24.Memory is arranged in
a. Liner fashion
b. Two dimensional manner page 396
c. Three dimensional manner
d. Random fashion

25. Which of the following output equations determines the output of the

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statemachine?

a. MIN = Q0Q1
b. MAX = Q0Q1EN page 382
c. MIN = Q0Q1EN
d. MAX = Q1EN

multiplexer with the register circuit convert

a. Serial data to parallel
b. Parallel data to serial page 349
c. Serial data to serial
d. Parallel data to parallel

27. The chip enable access time which is the timer for the validated data to appear after the____transition of the chip select signal CS

a. high to high
b. high to low page 397
c. low to high
d. low to low

28. The duration for which the elevator doors are opened , and remain open,, and time it takes for elevator to move from one floor to the next can be determined by a/an__

a. input signal
b. output signal
c. clock signal page 365
d. None of Given

29. The ABEL input file can use a_____instead of the equation to specify the Boolean expression

a. truth table page 370
b. state diagram
c. karnaugh map
d. logical circuit

30. Implementation of the FIFO buffer in RAM is usually takes the form of a _____buffer

a. Circular page 420
b. Rectangular
c. Triangular
d. Square

31. How many state variables does each state in Traffic Light Controller have?

a. One
b. Two

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c. Three page 377

d. Four

32. The output of SR latches in elevator state machine are generated bycombinational circuit therefore these output are defined as

ISTYPE_____

a. Com.reg

c. Com.buffer page 372

b. Com.org

d. Reg.buffer

33. When an eight bit serial in/out shift register is used for 24 micro second timedelay the clock frequency must be

a. 41.67 KHz

b. 333 KHs

c. 125 KHs

d. 8 MHz

34. Which of the following memories uses one transistor and one capacitor as basicmemory unit?

a. SRAM

b. DRAM page 400

c. PRAM

d. TRAM

35. A divide by 10 ring counter requires a minimum ofa. Ten flip flops

b. Five flip flops

c. Four flip flops

d. Twelve filp flops

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35. Which one flip flop has an invalid output state?

a. T

b. J

Kc.

SR

d. D

36. In the keyboard encounter how many times per second does the ring counter santhe keyboard

a. 600scans./seco

nb. 625 scan/second
c. 650 scan/second
d. 700 scan/second

37. Smallest unit of data
isa. a bit
b. a 4 bitnibbles
c. an 8 bit word
d. a 16 bit word

38. The output of SR latches in elevator state machine are feed back to the _____gate array for connection of D Flip Flops
a. NO
Tb. AND
c. OR
d. XOR

39. The static RAM(SRAM) is non-volatile and is not a_____density memory aslatch is required to store a single bit of information
a. Lo
wb. High
c. Medium
d. Hot

40. Choose the best possible answer of the following question.
The D flip flop is only activated by _____
a. A negative edged triggerb. A positive edged trigger
c. Both positive and negative edge triggered
d. None of the given options

41. The Fastmode page access allows_____memory read and access time when reading successive data values stored in connective locations on the samerow
a. Slo
w b. Faster
c. Medium
d. Modern

42. The next state table for REQ1, FLOOR1 and OPEN input indicates that the

_____can be pressed at any time either on the first floor orthe second floor inelevator

a. REQ0
b. Open
c. REQ1
d. FLOOR1

49.A 4-bit binary up/down counter in in the binary state of zero. The next state in the UP mode is?

☐ 0001
☐ 1000
☐ 1110
☐ 1111

50. In memory read cycle, the read cycle is initiated by

a. Providing data to the variable
b. Applying data to signals
c. Applying the address signals
d. Providing arithmetic operations

51. FLASH memory cell is implemented using a single floating gate _____ transistor

a. MOS
b. LOS
c. GOS
d. POS

52.UVEPROM is stands for

a. Ultra Variant
b. Ultra Vibrant
c. Ultra Violet
d. Ultra Visible

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53. Four 4k byte chips can be connected together to implement wordmemory

a. 10K
b. 15K
c. 16 K
d. 8K

54. There are_____basic typeof EPROM

a. Two
b. Three
c. Four
d. Five

55. Two type of memories namely the first in first out(FIFO) memory and last infirst out (LIFO) are implemented using _____
a. Shift Register
b. Circular Buffer
c. Ring Buffer
d. Reduce Registers

memory organized to store nibble data values requires a _____wide databus
- 2 bit
- 4 bit
  - 8 bit
- 16 bit

57. ROMs and PROMs retains information_____even if the supply voltage isremoved.
a. For one day
b. For seven days
c. Forten days
d. Permanently

58. You have to choose suitable option when your timer will reset by consideringthis given code:

```
TRSTATE.CLK = clk:
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);
```

a. NSY2 orEWY2
b. NSSR or TMRST
c. EWSR or NSRED
d. EWRed or EWYel

59. Synchronous SRAM uses a clock signal which is used by the tosynchronize its activities.
a. ALU
b. Control Unit
c. Microprocessor
d. Address Bus

60. Implementation of the FIFO buffer in_____is usually takes the form

of a circular buffer

a. RAM page 420
b. ROM
c. PROM
d. Flash Memory

The CONSTATE.CLK = Clock is used to indicate that the _ state variables change on a clock

57. The CONSTATE.CLK = Clock is used to indicate that the state variables change on a clock transition.
    a. CONSTATE
    b. FLOOR
    c. MOTION
    d. OPEN

58. The normal data inputs to a flip flop (D,S and R,J and K,T are referred) to as _____ inputs
    a. Sequential
    b. Asynchrono us
    c. Synchronous
    d. Combinational

59. The synchronous SRAM also has a burst feature which allows the synchronous SRAM to read or write up to location(s) using a single address
    a. One
    b. Two
    c. Three
    d. Four page 399

60. Two State variable allow maximum of _____ states
    a. Two
    b. Four page 381
    c. Eight
    d. Sixteen

61. Which of the following is the drawback of DRAM?
    a. Discharging of the capacitor over a period of time
    b. All the information stored in terms if binary bits would be lost if capacitor is not recharged

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c. Extra circuit is required to reference the capacitor

d. All of the above are true page 400

62. To write data to the memory the write cycle is initiated by

a. Applying the address signals 397

b. Assigning the values of variable

c. Reserving the space of variables

d. Applying the data signals

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