Cs 302 Mid Term Objective Type

Prepared By…….. ……..Talha Goraya

If you found any mistake plz feedback at
whatsapp 03401213047 & Email at
talhagoraya2000@gmail.com

Please choose one
A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► **When one or more product terms in the expression are equal to 1**

- Please choose one
The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► **A=01, B=10**

) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True**
► False

- Please choose one
High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► **0.9 V (**
► 3.3 V

Please choose one
If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them in
floating point representation and then multiplying them, the value of mantissa of result will be _____

► **24.582 (But not sure)**
► 2.4582
► 24582
► 0.24582

Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol“+“ here
represents OR Gate.

► Undefined
► **One**
► Zero

► 10 (binary)

Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET (
► RESET
► Clear
► Invalid

Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► Fast switching speeds, very low power dissipation
► Low switching speeds, very low power dissipation

Please choose one
The binary value “1010110” is equivalent to decimal _____

► 86 (According to Formula)
► 87
► 88
► 89

Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder

► BCD-to-Decimal
► **Decimal-to-BCD Priority**

Please choose one
"Sum-of-Weights" method is used _____

► **to convert from one number system to other (**
► to encode data
► to decode data
► to convert from serial to parralel data

- Please choose one
The maximum number that can be represented using unsigned octal system is _____

► 1
► **7**
► 9
► 16

- Please choose one
If we add “723” and “134” by representing them in floating point notation i.e. by first, converting them in
floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► **2**
► 3

Please choose one
The diagram given below represents _____

► Demorgans law
► Associative law
► **Product of sum form (According to rule of theorem)**
► Sum of product form

Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2**
► 1
► 3
► 4

- Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic**
► Generic Array Logic
► Generic Analysis Logic

- Please choose one
The Quad Multiplexer has _____ outputs

► **4**
► 8
► 12
► 16

Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan‟s Law
► Distributive Law
► Commutative Law

► **Associative Law (**

Please choose one
2's complement of any binary number can be calculated by

► adding 1's complement twice
► **adding 1 to 1's complement (**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Please choose one
The binary value “1010110” is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR (**

The binary value “11011” is equivalent to _____

►**1B (According to rule)**
►1C
►1D
►1E

. An important application of AND Gate is its use in counter circuit

►**True (**
►False

The OR Gate performs a Boolean _____ function

►**Addition**
►Subtraction
►Multiplication
►Division

TTL based devices work with a dc supply of ____ Volts

►+10
►**+5**
►+3
►3.3

A standard POS form has _____ terms that have all the variables in the domain of the expression.

►**Sum**
►Product
►Min
►Composite

. A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.

►2
►4
►**8 (According to rule)**

►16

A BCD to 7-Segment decoder has

►3 inputs and 7 outputs
►4 inputs and 7 outputs)
►7 inputs and 3 outputs
► inputs and 4 outputs

. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?

►A
► ►
C
►D

The binary value of 1010 is converted to the product term

►True
►False

10. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

►A > B = 1, A < B = 0, A < B = 1
►A > B = 0, A < B = 1, A = B = 0
►A > B = 1, A < B = 0, A = B = 0
►A > B = 0, A < B = 1, A = B = 1

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

►**SET ()**
►RESET
►Clear
►Invalid

. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS
5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal
(VoH) will be in the range of _____ volts.

►4 to 4.5
►**4.5 to 5**
►0 to 4.5
►0 to 3.5

. A.(B.C) = (A.B).C is an expression of _____

►Demorgan‟s Law
►Distributive Law
►Commutative Law
►**Associative Law**

The 4-bit 2's complement representation of "+5" is _____

►1010
►1110
►**1011**
►0101

Which of the number is not a representative of hexadecimal system

►1234
►ABCD

►1001

Please choose one

► 1
► **7**
► 9
► 16

- Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8**
► 12
► 16

Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output
levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0**
► A > B = 0, A < B = 1, A = B = 1

) - Please choose one
A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output
► 2 inputs and 3 output

► 2 inputs and 2 output

- Please choose one
The function to be performed by the processor is selected by set of inputs known as ____

► **Function Select Inputs**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?
► **2 (**
► 1
► 3
► 4

- Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (**
► Generic Array Logic
► Generic Analysis Logic

Please choose one
The Quad Multiplexer has _____ outputs
► **4**
► 8
► 12
► **16**

) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan‟s Law
► Distributive Law
► Commutative Law
► **Associative Law (**

- Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

- Please choose one
The binary value “1010110” is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

- Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► **NOT**
► **XOR**

- Please choose one
GALcan be reprogrammed because instead of fuses _____logic is

used in it

► **E2CMOS**
► TTL
► CMOS+
► **None of the given options**

Please choose one
The device shown here is most likely a

► Comparator
► **Multiplexer click here for detail**
► Demultiplexer
► Parity generator

Please choose one
If“1110” is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2nd
► 4th
► 14th
► **No output wire will be activated**

- Please choose one
Half-Adder Logic circuit contains 2 XOR Gates

► True
► **False**

- Please choose one
A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output

► 2 inputs and 3 output
► **2 inputs and 2 output**

- Please choose one
Sum = A ⊕ B ⊕ C CarryOut = C(A ⊕ B) + AB
are the Sum and CarryOut expression of

► Half Adder
► **Full Adder**
► 3-bit parralel adder
► MSI adder cicuit

Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input
variables and the resulting output of each value.

► **True click here for detail**
► **False**

Please choose one
The output A < B is set to 1 when the input combinations is

► A=10, B=01
► A=11, B=01
► A=01, B=01
► **A=01, B=10**

Please choose one
The 4-variable Karnaugh Map (K-Map) has _____cells for min or max terms

► 4
► 8
► 12

► **16**

- Please choose one
Generally, the Power dissipation of devices remains constant throughout their operation.

► **TTL**
► CMOS 3.5 series
► CMOS 5 Series
► **Power dissipation of all circuits increases with time.**

- Please choose one
The ecimal “8” is represented as using Gray-Code.

► 0011
► **1100**
► 1000
► 1010

Please choose one
(A+B).(A+C) =

► B+C
► **A+BC**
► AB+C
► AC+B

- Please choose one
A.(B+ C) = A.B + A.C is the expression of

► Demorgan‟s Law
► Commutative Law
► **Distributive Law**
► Associative Law

Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► **TRUE**

In ANSI/IEEE Standard 754 “Mantissa” is represented by 32-bits bits

► 8-bits
► 16-bits
► **32-bits**
► 64-bits

- Please choose one
Caveman number system is Base _5 number system

► 2
► **5**
► 10
► 16

- Please choose one
According to Demorgan‟s theorem:
_____

► A.B.C
►
► **(Page 74)**
►

- Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

\► 2-bit
► 7-bit
► 8-bit
► 16-bit

) - Please choose one
The AND Gate performs a logical _____function

► Addition
► Subtraction
► Multiplication
► Division

Please choose one
NOR gate is formed by connecting _____

► OR Gate and then NOT Gate
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► TTL
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True**
► False

Please choose one
When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► **NOT (**
► XOR

- Please choose one
The GAL22V10 has ____ inputs

► **22**
► 10
► 44
► 20

- Please choose one
The ABEL symbol for “OR” operation is

► !
► &
► **#**
► $

- Please choose one
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements**

► Depends on the type of PALs input size

Please choose one
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon)**
► " endl " (keyword "endl")

Please choose one
The Quad Multiplexer has _____ outputs

► **4 (**
► 8
► 12
► 16

- Please choose one
"Sum-of-Weights" method is used _____

► **to convert from one number system to other)**
► to encode data
► to decode data
► to convert from serial to parralel data

Please choose one
A latch has _____ stable states

► One
► **Two)**
► Three
► Four

- Please choose one
Sequential circuits have storage elements

► **True**
► False

Please choose one
The ABEL symbol for “XOR” operation is

► **$**
► #
► !
► &

- Please choose one
A Demultiplexer is not available commercially.

► **True**
► False

Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► **A parallel to serial converter circuit**
► A counter circuit
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

- Please choose one
The device shown here is most likely a
► Comparator
► **Multiplexer click here for detail**
► Demultiplexer

► Parity generator

Please choose one
The main use of the Multiplexer is to

► Select data from multiple sources and to route it to a single Destination (Page 167)
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

- Please choose one
A logic circuit with an output consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► two AND gates, one OR gate, two inverters
► two AND gates, one OR gate

Please choose one
The binary value of 1010 is converted to the product term

► True
► False

Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► 16

Please choose one
Following is standard POS expression

► **True (According to logic)**
► False

Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol"+" here
represents OR Gate.

► Undefined
► **One**
► Zero
► 10 (binary)

Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► **8-bit**
► 16-bit

- Please choose one
The diagram given below represents _____

► Demorgans law
► Associative law
► **Product of sum form (According to rule)**
► Sum of product form

Please choose one
The diagram given below represents _____

► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form**

Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Please choose one
The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► **16)**

Please choose one
A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► **4 inputs and 7 outputs**
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement

a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► **2-input, 4-bit**

- Please choose one
The PROM
consists of a fixed non-programmable _____ Gate array configured as a decoder.

► **AND**
► OR
► NOT
► XOR

Please choose one
In ABEL the variable „A“ is treated separately from variable „a“

► **True**
► False

Please choose one
The ABEL notation equivalent to Boolean expression A+B is:
► A & B
► A ! B
► **A # B**
► A $ B
L-21

Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be

_____.

► **SET**
► RESET
► Clear
► Invalid

Please choose one
Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs.**
► Multiple inputs and single output.

- Please choose one
Which one is true:

► **Power consumption of TTL is higher than of CMOS**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Please choose one
The first Least Significant digit in decimal number system has

position 0 and weight equal to 1
position 1 and weight equal to 0
position 1 and weight equal to 10
position 0 and weight equal to 10

Please choose one
The decimal equivalent of the binary number “10011” is

19 (According to rule)
99
29
None of given options

Please choose one
In ANSI/IEEE Standard 754 “Mantissa” is represented by 32-bits bits

► 8-bits
► 16-bits
► **32-bits**
► 64-bits

Please choose one
The binary value “11011” is equivalent to

1B (According to rule)
1C
1D
1E

- Please choose one
NOR gate is formed by connecting

OR Gate and then NOT Gate
NOT Gate and then OR Gate
AND Gate and then OR Gate
OR Gate and then AND Gate

- Please choose one
“74ALS” stands for

Advanced Low-frequency Schottky TTL
Advanced Low-dissipation Schottky TTL
Advanced Low-Power Schottky TTL

Advanced Low-propagation Schottky TTL

- Please choose one
An adder circuit can be used to perform subtraction operation

True
False

Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

2)
3 4 1

Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True
False

- Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a multiplexer.

2-input, 4-bit
4-input, 8-bit
4-input, 16-bit
2-input, 8-bit

Please choose one
The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected
together through a 4-input gate

AND
OR
NAND
XOR

- Please choose one
The Programmable Array Logic (PAL) has AND array and a OR array

Fixed, programmable
Programmable, fixed
Fixed, fixed
Programmable, programmable

Please choose one
Sequential circuits have storage elements

True
False

Please choose one
Demultiplexer has

Single input and single outputs.
Multiple inputs and multiple outputs.
Single input and multiple outputs.
Multiple inputs and single output.

Prepared By…….. ……..Talha Goraya

If you found any mistake plz feedback at
whatsapp 03401213047 & Email at
talhagoraya2000@gmail.com





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CS 302 GRAND QUIZ

Sr No.	MCQS QUESTION	ANSWER
1.	The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.	Faster
2.	In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.	NAND, NAND
3.	Why demultiplexer is called a data distributor?	Single input to Single Output
4.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input
5.	The n flip-flops store _____ states.	2^n
6.	The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.	NAND
7.	The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.	1
8.	As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.	Top
9.	In memory write cycle, the time for which the WE signal remains active is known as the _____.	Write pulse

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		width
10.	You have to choose suitable option when your timer will reset by considering this given code: TRSTATE.CLK = clk; TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);	NSY2 or EWY2
11.	Two signals _____ and _____ provide the timing inputs to the State Machine.	PTIME and QTIME
12.	PALs tend to execute _____ logic.	SOP
13.	Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?	-WE
14.	Memory is arranged in _____.	two-dimensional manner
15.	The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.	High
16.	Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.	8 AND

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17.	The maximum value, represented by a single hexadecimal digit is _____.	"F"
18.	The _____ input overrides the _____ input.	Asynchronous, synchronous
19	A SOP expression can be implemented by an _____ combination of gates.	AND-OR
20.	The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.	AND
21.	The Transition table is very similar to the _____ table.	State
22.	The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.	Truth Table
23.	A 3-variable karnaugh map has	eight cells
24.	If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.	Same
25.	Adding two octal numbers "36" and "71" result in _____.	127

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26.	Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.	One
27.	Subtractors also have output to check if 1 has been _____.	Primed
28.	Which of the following Output Equations determines the output of the State Machine?	MAX = Q0Q1EN
29.	When the transmission line is idle in an asynchronous transmission	It is set to logic high
30.	UVERPROM is stands for	Ultra-Voilet
31.	The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.	4
32.	Select the mode of programming in which GAL16V8 can be programmed:	All of the given
33.	The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.	CONSTATE
34	The domain of the expression AB'CD + AB' + C'D + B is	A, B, C and D

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35.	The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.	Small
36.	_____ Counters as the name indicates are not triggered simultaneously.	Synchronous
37.	The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.	Three
38.	The output of a NAND gate is _____ when all the inputs are one.	Zero
39.	For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.	1
40.	A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.	True
41.	Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.	Shift Registers
42.	The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.	XOR, NAND
43.	A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:	1111

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44.	Which of the following is a volatile memory?	DRAM
45.	The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.	REQ1
46.	The AND Gate performs a logical _____ function.	Division
47	Implementation of Latch is required almost _____ transistor.	Six
48.	Which one flip-flop has an invalid output state?	SR
49.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV 32
50.	The terminal count of a 4-bit binary counter in the UP mode is _____.	1100
51.	In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.	True
52.	The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.	Four
53.	Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.	RAM

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54.	An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.	Q output of all flip-flops to clock input of next flip-flops
55.	In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.	D(OUT)
56.	Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.	256
57.	8-bit parallel data can be converted into serial data by using _____ multiplexer.	8-to-1
58.	If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.	1001
59.	Canonical form is a unique way of representing _____.	SOP
60.	A NOR based S-R latch is implemented using _____ gates instead of _____ gates.	NOR, NAND
61.	Cin is part of _____ Adder.	Full
62.	Flash memory Operation are classified into _____ different operation.	Two

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63.	GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.	row, column
64.	In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.	7.8 microsec
65.	In the keyboard encoder, how many times per second does the ring counter scan the key board?	650 scans/second
66.	Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.	Negative-OR, Negative-AND
67	If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.	1
68.	The 64-cell array organized as 8 x 8 cell array is considered	as an 8 byte memory
69.	The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.	Synchronous
70.	PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.	PLDs

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71.	For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.	None of the given
72.	A multiplexer with a register circuit converts	Parallel data to serial
73.	The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.	Four
74.	Which of the following Output Equations determines the output of the State Machine?	MAX = Q0Q1EN
75.	8-bit parallel data can be converted into serial data by using _____ multiplexer.	8-to-1
76.	You have to choose suitable option when your timer will reset by considering this given code: TRSTATE.CLK = clk; TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);	NSY2 or EWY2
77.	UVERPROM is stands for	Ultra-Voilet
78.	In memory write cycle, the time for which the WE signal remains active is known as the _____.	Write pulse width

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79.	PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.	PLDs
80.	The Transition table is very similar to the _____ table.	State
81.	Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.	Negative-OR, Negative-AND
82.	The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.	CONSTATE
83.	Adding two octal numbers "36" and "71" result in	127
84.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV 32
85.	A multiplexer with a register circuit converts	Parallel data to serial
86.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input
87.	Memory is arranged in _____.	two-dimensional

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		manner
88.	Implementation of Latch is required almost _____ transistor.	Six
89.	In DRAM read cycle R /W- signal is activated to read data which is made available on the _____ data line.	D(OUT)
90.	Why demultiplexer is called a data distributor?	Single input to Single Output
91.	The maximum value, represented by a single hexadecimal digit is _____.	"F"
92.	Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.	RAM
93.	The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.	REQ1
94.	In a sequential circuit the next state is determined by _____ and _____	Current state and external input
95.	The divide-by-60 counter in digital clock is implemented by using two cascading counters:	Mod-6, Mod-10

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96.	The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop	Hold time
97.	74HC163 has two enable input pins which are _____ and _____	ENP, ENT
98	_____ is said to occur when multiple internal variables change due to change in one input variable	Race condition
99.	The _____ input overrides the _____ input.	Asynchronous, synchronous
100.	A decade counter is _____.	Mod-10 counter
101.	In asynchronous transmission when the transmission line is idle, _____	It is set to logic high
102.	A Nibble consists of _____ bits.	4

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103.	Excess-8 code assigns _____ to “-8”	0000
104.	The voltage gain of the Inverting Amplifier is given by the relation _____	Vout / Vin = - Rf / Ri
105.	LUT is acronym for _____	Look Up Table
106.	The three fundamental gates are _____	NOT, OR, AND
107.	The total amount of memory that is supported by any digital system depends upon _____	The size of the address bus of the microprocessor
108.	Stack is an acronym for_____	LIFO memory
109.	Addition of two octal numbers “36” and “71” results in _____	127
110.	._____ is invalid number of cells	J-K input

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	in a single group formed by the adjacent cells in K-map_____ is one of the examples of synchronous inputs.	
111.	_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	Clock Skew
112.	A GAL is essentially a _____.	Reprogrammable PAL
113.	_____, all the columns in the same row are either read or written.	FAST Mode Page Access
114.	In order to synchronize two devices that consume and produce data at different rates, we can use _____	Fist In First Out Memory
115.	A positive edge-triggered flip-flop changes its state when _____	Low-to-high transition of clock

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116.	A frequency counter _____	Counts no. of clock pulses in 1 second
117.	In a sequential circuit the next state is determined by _____ and _____	Input and clock signal applied
118.	Given the state diagram of an up/down counter, we can find ____	The next state of a given present state
119.	The total amount of memory that is supported by any digital system depends upon _____	The size of the address bus of the microprocessor
120.	The expression F=A+B+C describes the operation of three bits _____ Gate.	OR
121.	The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.	32-bit
122.	The basic building block for a logical circuit is _____	A Logical Gate
123.	The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.	Zero
124.	_____ is invalid number of cells in a single group formed by the adjacent cells in K-map.	12

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CS302 Digital Logic & Design

Grand Quiz Fall 2020

Department of MCS
Compose By
MUNIR HUSSAIN &
ASAD MUNIR
Semester 3rd

OBJECTIVE

1. A Product term is 0 when_____
   a. Any one literal is 0
   b. Any of the literals is 1
   c. At least two literals are 1
   d. All the literals are 1
2. In 8-inpit multiplexer, the two outputs are connected through a/an___gate.
   a. AND
   b. OR
   c. NOT
   d. NOR
3. ____ Device dissipate varying amount of power depending upon the frequency of operation.
   a. TTL
   b. CMOS
   c. Storage
   d. Peripheral
4. Boolean Addition operation is performed by a(an)___ gate.
   a. AND
   b. OR
   c. XOR
   d. NAND
5. A SOP expression can be implemented by an_____ combination of gates.
   a. OR-XOR
   b. AND-AND

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c. AND-OR
d. XOR-NOR

6. The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.
   a. 2^63
   b. (2^64)-1
   c. (2^64+
   d. 2^64
7. In 16-bit ALU, The G output is activated if the 4-bi unit generate a Carry ____ irrespective of Carry___.
   a. In,In
   b. In,Out
   c. Out,In
   d. Out,Out
8. A standard POS from has ____ ters that have all the variables in the domain of the expression.
   a. Sum
   b. Product
   c. Min
   d. Composite
9. In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles_____.
   a. Lower priority outputs
   b. Higher priority outputs
   c. Lower priority inputs
   d. Higher priority inputs
10. Which of the following is the example of comparater?
   a. OR
   b. AND
   c. XOR
   d. XNOR
11. IN CMOS 5 Volt series, Input voltage of Logic high signal (VIH) with a ranges from ____ to ____ volts.
   a. 4, 5, 5
   b. 0 ,5
   c. 0, 3, 5
   d. 3, 5, 5
12. The Adjacent 1 S Detector accepts 4-bits input. If ____ adjacent 1S are detected in the input, the output is set to high.
   a. 2
   b. 4

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c. 1
d. 0

13. DE Morgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.
    a. Negative-OR, Negative-AND
    b. Negative-AND, Negative-OR
    c. positive-OR, Negative-AND
    d. positive-AND, Negative-OR
14. Adding two octal numbers "36 and 71" result in ____.
    a. 213
    b. 123
    c. 127
    d. 345
15. Any of the _____ forms of the Karnaugh Map can be used to simplify Boolean expressions
    a. Three
    b. Four
    c. Two
    d. Five
16. Quine-McCluskey and K-Map methods are used for _____ of Boolean expression.
    a. Multiplication
    b. Addition
    c. Simplification
    d. Subtraction
17. The number "1259" may belong to ____ number system.
    a. Binary number system
    b. Octal or Decimal system
    c. Decimal or Hexadecimal system
    d. Binary or Hexadecimal system
18. The series of TTL chips are characterized by their____.
    a. Switching Speed only
    b. Power Dissipation only
    c. Both
    d. None of these
19. All ABEL statements must end with_____.
    a. :
    b. ,
    c. ;
    d. "

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20. In sequential circuit memory elements are connected with_____.
    a. Logical circuit
    b. Clock
    c. Feedback path
    d. External Event
21. In the 32-bit Single Precision Floating Point format, the exponent value_____ is reserved to represent infinity exponents.
    a. 98
    b. 99
    c. 255
    d. 256
22. The _____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.
    a. Combinational
    b. Combinational input/
    c. PLA
    d. None
23. The limitation in implementation of parallel binary address is known as_________.
    a. Delay
    b. Carry propagation
    c. Carry input
    d. Carry output
24. The Gray code is different form the unsigned binary code because___.
    a. Successive value of Gray code by only one bit
    b. Gray code is positional code
    c. Gray code not support negative values
    d. Gray code ranges from “o” to “9”
25. Removing the NOT gate at the output of the NOR gate result in an_____.
    a. OR gate
    b. NAND gate
    c. AND gate
    d. NOT gate
26. Portable devices that run on batteries use___ circuit that have low power dissipation.
    a. Series
    b. Integrated
    c. Parallel

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d. Electric

27. The domain of the expression AB'CD+B is
    a. A and D
    b. A,B,C and D
    c. C and D only
    d. B only

28. _____ is a single input gate
    a. AND
    b. OR
    c. NOT
    d. XOR

29. To represent in digital value, the number of digit (0s and 1s) that represent a quantity is _____ to the range of values that are to be represented.
    a. Equal
    b. Greater
    c. Lesser
    d. Not equal

30. BCD code of 16 is_____.
    a. 10001
    b. 00010001
    c. 00010111
    d. 01110001

31. To determine the seven expressions for each of the seven outputs in 7-segment display, seven____ variable Karnaugh Maps are used.
    a. 3
    b. 4
    c. 5
    d. 2

32. In Odd parity generator circuit which gate is used to detect parity errors?
    a. OR
    b. NOR
    c. XOR
    d. AND

33. A 3-variable Karnaugh map has
    a. Eight cells
    b. Three cells
    c. Sixteen cells
    d. Four cells

34. The measurable values generally change over a

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a. Specified period
b. Discrete range
c. Time
d. Continuous range

35. _____ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.
a. PAL
b. GAL
c. PLA
d. PROM

36. When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?
a. 1000
b. 1001
c. 1010
d. 1100

37. How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decorder?
a. One
b. Two
c. Three
d. Four

38. The simplified expression using either of the two K-maps are_____.
a. Similar
b. Different
c. Identical
d. None-identical

39. Which of the following expression in the product of sums form?
a. (A + B)(C+D)
b. (AB)(CD)
c. AB(CD)
d. AB + CD

40. CMOS technology is characterized by low power dissipation with_____ switching speeds.
a. Slow
b. Fast
c. Average
d. Medium

41. GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator
a. True

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b. False

42. High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____

a. 0.2 V
b. 0.5 V
c. 0.9 V
d. 3.3 V

43. The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol"+" here represents OR Gate

a. Undefined
b. One
c. Zero
d. 10(binary)

44. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

a. SET
b. RESET
c. Clear
d. Invalid

45. 3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

a. Low switching speeds, high power dissipation
b. Fast switching speeds, high power dissipation
c. Fast switching speeds, very low power dissipation (page61)
d. Low switching speeds, very low power dissipation

46. The binary value "1010110" is equivalent to decimal _____

a. 86
b. 87
c. 88
d. 89

47. The _____ Encoder is used as a keypad encoder.

a. 2-to-8 encoder
b. 4-to-16 encoder
c. BCD-to-Decimal
d. Decimal-to-BCD Priority

48. How many data select lines are required for selecting eight inputs?

a. 1
b. 2
c. 3
d. 4

49. The Quad Multiplexer has _____ outputs

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a. 4
b. 8
c. 12
d. 16

50. Demultiplexer has
a. Single input and single outputs.
b. Multiple inputs and multiple outputs.
c. Single input and multiple outputs.
d. Multiple inputs and single output.

51. The expression _____ is an example of Commutative Law for Multiplication.
a. AB+C = A+BC
b. A(B+C) = B(A+C)
c. AB=BA
d. A+B=B+A

52. The look-ahead carry circuits_____
a. Add a 1 to complemented inputs
b. Reduce propagation delay
c. Increase ripple delay
d. Determine sign and magnitude

53. What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?
a. B+C'D'+CD
b. B'+C'D'+CD
c. B+C'D'+C'D
d. B'+C'D'+CD'

54. 2-input, 8-bit Multiplexer, by setting the S input to logic_____ the____ inputs of both the multiplexers are selected.
a. Low
b. High, B
c. Low, C
d. Low, C

55. The maximum decimal number that can be represented using the 64-bit unsigned representation_____
a. 2^63
b. (2^64)-1
c. (2^64)+1
d. 2^64

56. When two or more products terms are assumed by Boolean addition, the result is a ____
a. POS

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b. SOP
c. Boolean
d. Simplified

57. Tri-State Buffer is a ___ gate with a control line that disconnects the
a. OR
b. AND
c. NAND
d. NOT

58. The 4-bits 2's complement representation of "7" is _____
a. 0111
b. 1111
c. 1001
d. 0110

59. _____and _____ are the steps of the Quine-McCluskey.
a. Draw a table and make groups
b. Write binary codes and write SOP
c. Find prime implicants and select minimal set of the prime implicants.
d. None of the given

60. The binary number 1011,101 has an Integer part represented by_____ and a fraction part ___ separated by a decimal point.
a. 1011,101
b. 101,1011
c. 101,1101
d. 10111,11

61. Subtractors also have output to check if 1 has been _____
a. Primed
b. Shifted
c. Complemented
d. Borrowed

62. CMOS technology is characterized by low power dissipation with_____ switching speeds.
a. Slow
b. Fast
c. Average
d. Medium

63. The _____ description is used to simulate the logic circuit and verify its operation.
a. Test file

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b. Declaration
c. Logic
d. Test vector

64. How many outputs can an integrated circuit comparator have?
a. One
b. Two
c. Three
d. Four

65. Which of the following is not the correct method of grouping?
a. Along adjacent columns
b. On comers
c. Diagonally
d. Along adjacent rows

66. The output of the expression F=A.B.C will be logic _____ when A=1,B=0, C=1.
a. Undefined
b. One
c. Zero
d. No output as input is valid

67. The _____ gate and ___ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.
a. AND,NOR
b. AND,NOT
c. AND,OR
d. XOR,NAND

68. In the 32-bit Single Precision Floating point format, the exponent value _____ is reserved infinity exponent.
a. 98
b. 99
c. 255
d. 256

69. The Boolean expression (AB'CS') is used
a. A sum term
b. A product term
c. A literal term
d. A max term

70. The product of an XOR gate is zero(0), when _____
I. All the inputs are zero

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II. Any of the inputs is zero
III. An of the inputs is one
IV. All the inputs are one

a. I only
b. IV only
c. I and IV only
d. II and III

71. _____ methods are used to Convert Decimal fractions to Binary.
a. 1
b. 2
c. 3
d. 4

72. To display the number___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit
a. 19
b. 29
c. 39
d. 49

73. The look-ahead carry circuits_____
a. Add a 1 to complemented inputs
b. Reduce propagation delay
c. Increase ripple delay
d. Determine sign and magnitude.

74. If two numbers in BCD representation generate an invalid BCD number then the binary __ is added to the result
a. 1001
b. 0110
c. 1111
d. 1100

75. Both the multiplexers are selected simultaneously when _____ is set to logic _____ in 2-inputs, 8-bit Multiplexer.
a. G, Low
b. G, High
c. S, Slow
d. S, High

76. Function labels required to represent the input/output combinations for each segment in 7-segment display
a. 5
b. 7

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c. 8
d. 10

77. Multiplexers are also known as _____
a. Date distributors
b. Data selectors
c. Data manipulators
d. Data setters

78. The PLA can be programmed to give and output of constant _____ or _____
a. 0,1
b. 1,2
c. 2,3
d. 0,0

79. Cin is part of _____ Adder.
a. Half
b. Full
c. Single
d. Double

80. The look-ahead carry circuits_____
a. Add 1 to complemented inputs
b. Reduce propagation delay
c. Increase ripple delay
d. Determine sign and magnitude

81. Which of the following gates has the outputs 1 if and only if at last one input is 1?

a. AND
b. NOR
c. NAND
d. OR

82. A sop expression can be implemented by on ___ combination of gates.
a. OR-XOR
b. AND-NAND
c. AND-OR
d. XOR-NOR

83. The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through ___ ALU units in 16-bit ALU.
a. Two
b. Four

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c. Eight
d. Sixteen

84. High level noise margins(VNH) of CMOS 5 volt series circuits is_____
a. 0.3 V
b. 0.5 V
c. 0.9 V
d. 3.3 V

85. Combinational Logic is used for combinational circuits, whereas Registered Logic is based on_____
a. Single
b. Multiple
c. Consecutive
d. Sequential

86. A specific half-adder has____ inputs and ___ outputs(s).
a. 3,1
b. 3,2
c. 2,1
d. 2,2

87. The OR Gate performs a Boolean_____ function
a. Addition
b. Subtraction
c. Multiplication
d. Division

88. In 16-input multiplexer, the decoder inputs____ and___ enable one out of the four multiplexers.
a. A,B
b. B,C
c. C,D
d. A,D

89. IN CMOS 5 Volt, input voltage of Logic high signal(VIH) with a ranges from _____ to___ volts.
a. 4.5,5
b. 0,5
c. 0,3.5
d. 3.5,5

90. How many maximum groups can be generated in 3 variable K amp?
a. 3
b. 6
c. 8

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d. 9

91. Digital circuits operates with_____ voltage value(s)
    a. 1
    b. 2
    c. 3
    d. 4

92. Which of the following is the octal equivalent of 28 decimal numbers?
    a. 31
    b. 32
    c. 33
    d. 34

93. In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles_____
    a. Lower priority outputs
    b. Higher priority outputs
    c. Lower priority inputs
    d. Higher priority inputs

94. To determine the seven expressions for each of the seven outputs in 7-segment display, seven _____ variable Karnaugh maps are used.
    a. 3
    b. 4
    c. 5
    d. 2

95. The output of a NAND Gate is ____ when all the inputs are one.
    a. Zero
    b. One
    c. Available
    d. Not available

96. The _____ is the slowest and consumes more power.
    a. Standard TTL
    b. Schottky TTL
    c. Advanced Schokottky TTL
    d. Low-Power Schottky TTL

97. The between expression X-AB+CD represents
    a. Two Ors ANDed together
    b. A 4-input AND gate
    c. Two ANDs ORed together
    d. An eclusive-OR

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98. The expression F-A+B+C describes the operation of three bits___ Gate.
   a. OR
   b. AND
   c. NOT
   d. NAND
99. Which one of the following is NOT a valid rule of Boolean Algebra?
   a. A+1=1
   b. A=A'
   c. AA=A
   d. A+0=A
100. A 5-Variable Karnaugh map has
   a. Sixteen cells
   b. Thirty two cells
   c. Sixty four cells
   d. None of these
101. ____ is invalid number of cells in a single group formed by the adjacent cells K-map
   a. 2
   b. 8
   c. 12
   d. 16
102. In 32-bit Single -Precision floating point format representation the range of exponent value is from _____to _____
   a. +127 to -126
   b. +127 to -254
   c. +128 to -254
   d. +256 to -255
103. ____ has the fastest switching speed and low power requirements
   a. Advanced low power schottky
   b. Fast TTL
   c. Standard TTL
   d. Schottky TTL

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Digital Logic Design CS302

Lecture No 1

Digital representing of quantities

Digital quantities unlike Analogue quantities are not continuous but represent quantities measured at discrete intervals.

Electronic Processing of Continuous and Digital Quantities

Electronic Processing of the continuous quantities or their Digital representation requires that the continuous signals or the discrete values be converted and represented in terms of voltages. There are basically two types of Electronic Processing Systems.

- **Analogue Electronic Systems:** **Digital Electronic Systems:**

Digital Systems and Digital Values

Digital systems are designed to work with two voltage values. A +5 volts represents a logic high state or logic 1 state and 0 volts represents a logic low state or logic 0 state.

Digital Systems are based on the Binary Number system which allows more than two or multiple values to be represented very conveniently.] Any quantity can be represented through digital values. The number of digits (0s and 1s) that represents a quantity is proportional to the range of values that are to be represented. Computers process information that is represented digitally in the form of Binary Numbers.

Data can be easily and precisely reproduced: The picture quality and the sound quality of digital videos are far more superior to those of analogue videos. The reason being that the digital video stored as digital numbers can be exactly reproduced whereas analogue video is stored as a continuous signal cannot be reproduced with exact precision.

Digital circuits occupy small space: Digital circuits are based on two logical states. Characters used in writing text are represented through yet another standard known as ASCII which allows alphabets, punctuation marks and numbers to be represented through a combination of 0s and 1s. Large and complex digital system such as a computer is built using combinations of these basic Logic Gates. These basic building blocks are available in the form of Integrated Circuit or ICs.

Combinational Logic Circuits and Functional Devices

The logic gates which form the basic building blocks of a digital system are designed to perform simple logic operations. Digital circuits that generate a new output on the basis of some previously stored information and the new input are known as Sequential circuits.

PLD Programmable Logic Devices can be used to implement Combinational and Sequential Digital Circuits.

RAM and ROM are an essential part of a digital system.

Caveman number system

A number system discovered by archaeologists in a prehistoric cave indicates that the caveman used a number system that has 5 distinct shapes Σ, Δ, >, Ω and ↑.

Lecture No 2

Binary to Decimal conversion

Most real world quantities are represented in Decimal Number System. Digital Systems on the other hand are based on the Binary Number System. Therefore, when converting from the Digital Domain to the real-world, Binary numbers have to be represented in terms of their Decimal equivalents.

There are two methods to convert binary to decimal.

1. **Sum-of-Weights Method**
2. **Sum-of-non-zero terms**
   The Sum-of-non-zero terms method is a quicker method to determine decimal equivalents of binary numbers without resorting to writing an expression.

Decimal to Binary conversion:

The **Sum-of-weights** and **repeated division by 2** methods are used to convert a Decimal number to equivalent Binary.

Sum-of-weights

43_{10}

H Weight	64	32	16	8	4	2	1
Binary Num		1	0	1	0	1	1_2

A Binary 1 is marked to represent the bit which contributed its weight in the Sum representing the decimal equivalent. The weight is subtracted from the sum decimal equivalent. The next highest weight included in the sum term is found. A binary 1 is marked to represent the bit which contributed its weight in the sum term and the weight is subtracted from the sum term. This process is repeated until the sum term becomes equal to zero.

Converting Decimal fractions to Binary:

Repeated Multiplication-by-2 Method:

In this method the number to be converted is repeatedly multiplied by the Base Number to which the number is being converted to, in this case 2. A new number having an Integer part and a Fraction part is generated after each multiplication. The Integer part is noted down and the fraction part is again multiplied with the Base number 2. The process is repeated until the fraction term becomes equal to zero.

Binary Arithmetic

Digital systems use the Binary number system to represent numbers. Therefore, these systems should be capable of performing standard arithmetic operations on binary numbers.

Binary Multiplication by shifting left

00011 (3) original binary number
00110 (6) binary number shifted left by 1 bit
01100 (12) binary number shifted left by 2 bits
11000 (24) binary number shifted left by 3 bits

Binary Division by Shifting right

10100 (20) original binary number
01010 (10) binary number shifted right by 1 bit
00101 (5) binary number shifted right by 2 bits

Signed and Unsigned Binary Numbers

Digital systems not only handle positive numbers but both positive and negative numbers. In a digital system which uses the Binary number system, the positive and negative signs cannot be represented as + and -. As mentioned in the Overview all forms of numbers, text, punctuation marks etc. are represented in the form of 1s and 0s. Thus the positive and negative signs are also presented in terms of binary 0 and 1.

MSB set to 1 indicates a negative number **MSB set to 0 indicates a positive number**

Thus +13 and -13 are represented as 01101and 11101 respectively. The bits 1101 represent the number 13 and the MSBs 0 and 1 represent positive and negative signs respectively.

1's & 2's complement

Informing the digital system how to treat a binary number is not very efficient. A better way is to represent negative signed numbers in their 2's complement form.

01101 The number 13
10010 1's complement of 13 is obtained by inverting all the five bits.
+ 1
(The num is -13) 10011 2's complement of 13 is obtained by adding a 1 to its 1's complement.

In a 2's complement number system all negative numbers are represented in their 2's complement form and all positive numbers are represented in their actual form.

Addition and Subtraction Operations with Signed Binary

An additional benefit of using 2's complement representation for signed numbers is that both add and subtract operations can be performed by addition.

Range of Signed and Unsigned Binary numbers

Three different types of Binary representations have been discussed. The Unsigned Binary representation can only represent positive binary numbers. The Sign-Magnitude can represent both positive and negative numbers. The 2's complement signed representation also allows positive and negative numbers to be handled.

Lecture No 3

Range of Numbers and Overflow

When arithmetic operation such as Addition, Subtraction, Multiplication and Division are performed on numbers the results generated may exceed the range of values specified by the Binary representations. The values that exceed the specified range cannot be correctly represented and are considered as Overflow values.

Determining Overflow Conditions for 2's Complement Numbers

The Overflow condition can be easily determined when two numbers represented in 2's Complement form are added together.

Floating-Point Numbers

Modern computers can handle large binary numbers such as 64-bit unsigned number, the maximum decimal number that can be represented using the 64-bit unsigned representation is 2^{64}-1 which is nearly equal to1.84×10^{19}.
The number 6918.3125 can be written as 6.9183125×10^{3}.

Arithmetic Operations on Floating Point Numbers

Arithmetic operations can be directly performed on floating point numbers by manipulating the mantissa and exponent parts of the floating point numbers.

723 represented in f.p. as exponent 2 mantissa 7.23
+ 134 represented in f.p. as exponent 2 mantissa 1.34

857 Adding together the mantissa part results in exponent 2 mantissa 8.57

Hexadecimal Numbers

The Hexadecimal number system is a base 16 number system and therefore has 16 digits and is used primarily to represent binary strings in a compact manner. Hexadecimal number system is not used by a Digital System. The Hexadecimal number system is for our convenience to long binary strings in a short and concise form. Each Hexadecimal Number digit can represent a 4-bit Binary Number.

Binary to Hexadecimal Conversion

Converting Binary to Hexadecimal is a very simple operation. The Binary string is divided into small groups of 4-bits starting from the least significant bit. Each 4-bit binary group is replaced by its Hexadecimal equivalent.

11010110101110010110	Binary Number
1101 0110 1011 1001 0110	Dividing into groups of 4-bits
D 6 B 9 6	Replacing each group by its Hexadecimal equivalent

Hexadecimal to Binary Conversion

Converting from Hexadecimal back to binary is also very simple. Each digit of the Hexadecimal number is replaced by an equivalent binary string of 4-bits.

FD13	Hexadecimal Number
1111 1101 0001 0011	Replacing each Hexadecimal digit by its 4-bit binary equivalent

Decimal to Hexadecimal Conversion

There are two methods

1. Indirect Method

A decimal number can be converted into its Hexadecimal equivalent indirectly by first converting the decimal number into its binary equivalent and then converting the binary to Hexadecimal.

2. Repeated Division-by-16 Method

The decimal number is continuously divided by 16 (base value of the Hexadecimal number system).

Lecture No 4

Octal Numbers

Octal Number system also provides a convenient way to represent long string of binary numbers. The Octal number is a base 8 number system with digits ranging from 0 to 7. Each Octal Number digit can represent a 3-bit Binary Number.

Binary to Octal Conversion

Converting Binary to Octal is a very simple. The Binary string is divided into small groups of 3-bits starting from the least significant bit. Each 3-bit binary group is replaced by its Octal equivalent.

11101011010111001011 0							Binary Number
111	010	110	101	110	010	110	Dividing into groups of 3-bits
7	2	6	5	6	2	6	Replacing each group by its Octal equivalent

Octal to Binary Conversion

Converting from Octal back to binary is also very simple. Each digit of the Octal number is replaced by an equivalent binary string of 3-bits

1726 Octal Number				
001	111	010	110	Replacing each Octal digit by its 3-bit binary equivalent

Working with different Binary representations

There are different ways of representing numbers in binary. Four ways of representing binary numbers have been already discussed.

- Unsigned binary
- Signed-Magnitude form
- 2's Complement form
- Floating point notation

Alternate forms of Binary representations

There are many different ways to represent binary numbers, other than the 4 representation

Many of these alternate representations are used to support specific applications and requirements.

The Excess Code

Consider the decimal number range +7 to -8. These positive and negative decimal numbers can be represented by the 2's complement representation. The magnitude of positive and negative numbers cannot be easily compared as the positive and negative numbers represented in 2's complement form are not represented on a uniformly increasing scale.

The BCD Code

Binary Coded Decimal (BCD) code is used to represent decimal digits in binary. BCD code is a 4-bit binary code; the first 10 combinations represent the decimal digits 0 to 9. Remaining six 4-bit combinations 1010, 1011, 1100, 1101, 1110 and 1111 are considered to be invalid and do not exist.
A telephone keypad having the digits 0 to 9 generates BCD codes for the keys pressed.

The Gray Code

The Gray code does not have any weights assigned to its bit positions. The Gray Code is not a positional code. The Gray code is different from the unsigned binary code as successive values of Gray code differ by only one bit.

Alphanumeric Codes

All the representation studied so far allow decimal numbers to be represented in binary. Digital systems also process text information as in editing of documents. Thus each letter of the alphabet, upper case and lower case, along with the punctuation marks should have a representation. Numbers are also written in textual form such as 2nd June 2003. The ASCII Code is a universally accepted code that allows 128 characters and symbols to be represented.

ASCII Code

The ASCII Code (American Standard Code for Information Interchange) is a 7-bit code representing 128 unique codes which represent the alphabet characters A to Z in lower case and upper case, the decimal numbers 0 to 9, punctuation marks and control characters.

Extended ASCII Code

The 7-bit ASCII code only has 128 unique codes which are not enough to represent some graphical characters displayed on Computer screens. An 8-bit code Extended ASCII code gives 256 unique codes. The extended 128 unique codes represent graphic symbols which have become an unofficial standard as vendors use their own interpretation of these graphic codes.

Parity Method

Binary information which can be text or numbers is processed, stored and transmitted. Although digital systems are extremely reliable but still there is a possibility that one bit gets corrupted. That is, a 1 changes to 0 or 0 changes to 1. Many systems use a parity bit to detect errors. A single parity based error detection scheme is not very practically efficient and more elaborate and robust schemes have been designed and implemented to detect and correct multiple bit errors.

Even Parity Method

The information 10001101 is to be transmitted to a remote location. A parity bit error detection method is adopted to indicate if the information has been corrupted when it reaches the other end. In the Even Parity method the number of 1s is counted in the information and depending upon the number of 1s in the message the appended parity bit is either set to 0 or 1 to make the total number of 1s to be even (Even Parity)

Lecture No 5

LOGIC GATES

The Digital Systems should be able to process or perform operations on the numbers that are represented in the Binary Number System.
Digital Logic Gates provide the basic building blocks; these Logic Gates perform different operations on the Binary information. These Logic Gates are used in different combinations to implement large complex systems. Digital Logic Gates are represented and identified by unique symbols. These symbols are used in circuit diagrams to describe the function of a digital circuit.

AND Gate

The AND Gate performs a logical multiplication function. An AND Gate has multiple inputs and a single output.
OR Gate: The OR Gate performs a Boolean add function. An OR Gate has multiple inputs and a single output. Most commonly used OR Gates are two input OR gates.
NOT Gate: NOT Gate is also known as an Inverter. The name indicates that the NOT Gate should be performing an inversion function. The Not Gate has a single input and a single output.
NAND Gate: The NAND Gate performs a function that is equivalent to the function performed by the combination of an AND gate and a NOT gate. A NAND Gate has multiple inputs and a single output.

NAND Gate as a Universal Gate

The NAND gate is also used as a Universal Gate as the NAND Gate can be used in a combination to perform the function of a AND, OR and NOT gates.

1. NOT Gate

Implementation: A NOT gate can be implemented using a NAND gate by connecting both the inputs of the NAND gate together. By connecting the two inputs together, the input combinations where the inputs are dissimilar become redundant.

2. AND Gate Implementation

A NAND Gate performs the AND-NOT function. Removing the NOT gate at the output of the NAND gate results in an AND gate. The effect of the NOT gate at the output of the NAND gate can be cancelled by connecting a NOT gate at the output of the NAND Gate.

3. OR Gate Implementation

An OR Gate can be implemented using a combination of three NAND gates. The implementation is based on the alternate symbolic representation of the OR gate. The OR gate is represented as an AND gate with bubbles at the inputs and outputs.

NOR Gate

The NOR Gate performs a function that is equivalent to the function performed by a combination of an OR gate and a NOT gate.

Lecture No 6

NOR Gate as a Universal Gate

The NOR gate is also used as a Universal Gate as the NOR Gate can be used in a combination to perform the function of a AND, OR and NOT gates.

NOT Gate Implementation

A NOT gate can be implemented using a NOR gate by connecting both the inputs of the NOR gate together. By connecting the two inputs together, the combinations with dissimilar inputs become redundant.

OR Gate Implementation

A NOR Gate performs the OR-NOT function. Removing the NOT gate at the output of the NOR gate results in an OR gate. The effect of the NOT gate at the output of the NOR gate can be cancelled by connecting a NOT gate at the output of the NOR Gate. The two NOT gates cancel each other out.

AND Gate implementation

An AND Gate can be implemented using a combination of three NOR gates. The implementation is based on the alternate symbolic representation of the AND gate. The AND gate is represented as an OR gate with bubbles at the inputs and outputs.

NAND-NOR Universal Gates

NAND and NOR gates are known as Universal Gates as they can be used to implement any of the three fundamental gates, AND, OR and NOT.

NAND gate Implementation using NOR gates

A NAND gate implementation requires addition of an inverter (NOT) gate at the output. The NOT gate is implemented using a NOR gate.

NOR gate Implementation using NAND gates

A NOR gate implementation requires addition of an inverter (NOT) gate at the output. The NOT gate is implemented using a NAND gate.

NAND and NOR Gate Applications

The output of a NAND is 0 when all inputs to the NAND gate are 1s. This property of the NAND gate can be used to activate an operation when any of the inputs to the NAND gate are deactivated. A NOR gate on the other hand generates an output of 1 when all inputs to NOR gate are deactivated. The output is deactivated when any input is activated.

Exclusive-OR Gate

The Exclusive-OR Gate or XOR Gate performs a function that is equivalent to the combination of NOT, AND and OR gates. XOR gates are extensively used in digital applications;

Logical XOR Operation

Inputs Output 0 0 = 0, 0 1 = 1, 1 0 = 1, 1 1 = 0

Exclusive-NOR Gate

The Exclusive-NOR Gate or XNOR Gate performs a function that is equivalent to the combination of NOT, AND and OR gates. XNOR gate is extensively used in digital applications;

Logical XOR Operation

Inputs Output 0 0 = 1, 0 1 = 0, 1 0 = 0, 1 1 = 1

XOR and XNOR Gate Applications

XOR and XNOR gates are used to detect dissimilar and similar inputs. This property of XOR and XNOR gates is used to detect odd and even number of 1s in a Parity Detection Circuit.

TTL/CMOS NOT Gate Operation

Logic Gates are implemented using transistors. These transistors are connected in various combinations to form a switching circuit. The transistor itself is configured to work like a switch. On the application of a bias voltage the transistor is switched on and by removing the bias voltage the transistor is turned off.

Lecture No 7

DC Supply Voltage: TTL based devices work with a dc supply of +5 Volts. TTL offers fast switching speed,

Immunity from damage due to electrostatic discharges. Power consumption is higher than CMOS. The TTL family has six different types of devices characterized by different power dissipation and switching speeds. The series of TTL chips are:

- 74 Standard TTL
- 74S Schottky TTL
- 74AS Advanced Schottky TTL
- 74LS Low-Power Schottky TTL
- 74ALS Advanced Low-Power Schottky TTL
- 74F Fast TTL

The Standard TTL is the slowest and consumes more power and the Advanced low power Schottky has the fastest switching speed and low power requirements.

CMOS technology is the dominant technology today and used in large scale ICs and microprocessors. CMOS technology is characterized by low power dissipation with slow switching speeds. There are two categories of CMOS in terms of the dc supply voltage. The 3.3 v CMOS series is characterized by fast switching speeds and very low power dissipation as compared to the 5 v CMOS series.

- +5 V CMOS
  - o 74HC and 74HCT High-Speed
  - o 74AC and 74ACT Advanced CMOS
  - o 74AHC and 74AHCT Advanced High Speed
- 3.3 V CMOS
  - o 74LV Low voltage CMOS
  - o 74LVC Low-voltage CMOS
  - o 74ALVC Advanced Low voltage CMOS

Logic Levels and Noise Margin: The TTL and CMOS circuit operating at +5 or 3.3 Volts respectively are designed to accept voltages in a certain range as logic 1 and 0.

Noise Margin Noise margin is a measure of the circuit's immunity to noise. The high-level and low level noise margins are represented by V_{NH} and V_{NL} respectively.

The CMOS 5 volts and the 3.3 volts series cannot be mixed.

For CMOS 5 volt series the high-level noise margin is 0.9 volts. That is, the logic high output of the gate would never be below 4.4 volts.

The V_{NH} high-level and V_{NL} low-level noise margins for TTL 5 volt and CMOS 3.3 series are 0.4 volts and 0.4 volts respectively. Therefore in noisy environments, CMOS 5 volt series based digital system perform better.

Power Dissipation: Logic Gates and Logic circuits consume varying amount of power during their operation. Ideally, logic gates and logic circuit should consume minimal power. Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries use Integrated circuits that have low power dissipation. Secondly, low power consumption means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices. Microprocessors for example generate considerable heat which has to be dissipated by mounting small fans.

Generally, the Power dissipation of TTL devices remains constant throughout their operation. CMOS device on the other hand dissipate varying amount power depending upon the frequency of operation.

Power Dissipation of TTL Devices: When a TTL logic gate output is in a logic high state it draws out a current from the dc power supply. It is said to be sourcing current. The high current is designated by I_{CCH}, typical value for I_{CCH} is 1.5 mA when V_{CC} = 5 V. When a TTL logic gate output is in a logic low state it sinks a current designated by I_{CCL} = 3.0 mA when V_{CC} = 5 V.

Power Dissipation in TTL circuits is constant over its range of operating frequencies. For example, the power dissipation of a LS TTL gate is a constant 2.2 mW.

Power Dissipation of CMOS Devices: The transistors used in CMOS logic present a capacitive load instead of the resistive load in TTL based logic. Each time a CMOS logic gate switches between low and high, current has to be supplied to the capacitive load. The typical supply current is 5 mA for a duration of 20-30 nsec. As the frequency of operation increases, there would be more of these current spikes occurring per second, thus the average current drawn from the voltage source increases. Power Dissipation in CMOS circuits is frequency dependent. It is extremely low under static (dc) conditions and increases as the frequency increases. Total Dynamic Power dissipation of a CMOS circuit is $P_D = P_T + P_L$

Propagation Delay: Whenever a signal passes through a gate it experiences a delay. That is, a signal applied to the input of a gate does not result in an instantaneous response. The output of a gate is delayed with respect to the input. The delay in the output is known as the Propagation Delay.

Speed-Power Product (SPP): An important parameter is the Speed-Power Product which is used as a measure of performance of a logic circuit taking into account the propagation delay and the power dissipation.

Fan-Out and Loading: The fan-out of a logic gate is the maximum numbers of inputs of the same series in an IC family that can be connected to a gate's output and still maintain the output voltage levels within the specified limits. Fan-out parameter is associated with TTL technology. CMOS circuits have very high impedance therefore fan-out of CMOS circuits is very high but depends upon the frequency because of capacitance effects.

Lecture No 8

Any digital circuit no matter how complex can be described by Boolean Expressions. Boolean algebra is the mathematics of Digital Systems. Knowledge of Boolean algebra is indispensable to the study and analysis of logic gates. AND, OR, NOT, NAND and NOR gates perform simple Boolean operations and Boolean expressions represent the Boolean operations performed by the logic gates.

• AND gate F = A.B • OR gate F = A + B • NOT gate F = $\overline{A}$

• NAND gate F = $\overline{A.B}$ • NOR gate F = $\overline{A + B}$

Boolean Algebra expressions are written in terms of variables and literals using laws, rules and theorems of Boolean Algebra. Simplification of Boolean expressions is also based on the Boolean laws, rules and theorems.

Boolean Algebra Definitions

1. Variable: A variable is a symbol usually an uppercase letter used to represent a logical quantity. A variable can have a 0 or 1 value.

2. Complement: A complement is the inverse of a variable and is indicated by a bar over the variable. Complement of variable X is $\overline{X}$. If X = 0 then $\overline{X}$ = 1 and if X = 1 then $\overline{X}$ = 0.

3. Literal: A Literal is a variable or the complement of a variable.

Boolean Addition: Boolean Addition operation is performed by an OR gate. In Boolean algebra the expression defining Boolean Addition is a sum term which is the sum of literals.

A + B, $\overline{A}$ + B, A + $\overline{B}$ + C

• A sum term is 1 when any one literal is a 1 • A sum term is 0 when all literals are a 0.

Boolean Multiplication: Boolean Multiplication operation is performed by an AND gate. In Boolean algebra the expression defining Boolean Multiplication is a product term which is the product of literals.

A.B , $\overline{A}$.B , A.B.C

• A product term is 1 when all literal terms are a 1 • A product term is 0 when any one literal is a 0.

Laws of Boolean Algebra: The basic laws of Boolean Algebra are the same as ordinary algebra and hold true for any number of variables.

1. Commutative Law for addition and multiplication A + B = B + A A.B = B.A
2. Associative Law for addition and multiplication A + (B + C) = (A + B) + C A.(B.C) = (A.B).C
3. Distributive Law A.(B + C) = A.B + A.C

Rules of Boolean Algebra: Rules of Boolean Algebra can be proved by replacing the literals with Boolean values 0 and 1.

1. A + 0 = A 2. A + 1 = 1 3. A.0 = 0 4. A.1 = A 5. A + A = A 6. A + $\overline{A}$ = 1 7. A.A = A
8. A.$\overline{A}$ = 0 9. $\overline{\overline{A}}$ = A 10. A + A.B = A = A.(1 + B)

Demorgan's Theorems: Demorgan's First Theorem states: The complement of a product of variables is equal to the sum of the complements of the variables.

$\overline{A.B}$ = $\overline{A}$ + $\overline{B}$

DE Morgan's Second Theorem states: The complement of sum of variables is equal to the product of the complements of the variables.

$\overline{A + B}$ = $\overline{A}$.$\overline{B}$

Standard Form of Boolean Expressions: All Boolean expressions can be converted into and represented in one of the two standard forms

• Sum-of-Products form • Product-of-Sums form

1. Sum of Product form: When two or more product terms are summed by Boolean addition, the result is a Sum-of-Product or SOP expression.

• AB + ABC • ABC + CDE + BCD • AB + ABC + AC

2. Product of Sums form: When two or more sum terms are multiplied by Boolean multiplication, the result is a Product-of-Sum or POS expression.

• (A + B)(A + B + C) • (A + B + C)(C + D + E)(B + C + D) • (A + B)(A + B + C)(A + C)

Conversion of a general expression to SOP form: Any logical expression can be converted into SOP form by applying techniques of Boolean Algebra.

• AB+ B(CD + EF) = AB+ BCD + BEF
• (A + B)(B + C + D) = AB+ AC+ AD+ B + BC + BD = AC+ AD+ B
• (A + B) + C = (A + B)C = (A + B)C = AC + BC

Lecture No 9

BOOLEAN ALGEBRA AND LOGIC SIMPLIFICATION

Boolean Analysis of Logic Circuits, evaluating of Boolean expressions, representing the operation of Logic circuits and Boolean expressions in terms of Function tables and representing Boolean expressions in SOP and POS forms are inter-related. Boolean laws, rules and theorems are used to readily change from one form of representation to the other.

The output of the logic circuit is 1 when X = 0 and Y = 0

- X=0 NOR Y=0 Output = 1
- X=0 NOR Y=1 Output = 0
- X=1 NOR Y=0 Output = 0
- X=1 NOR Y=1 Output = 0

Standard SOP form

A standard SOP form has product terms that have all the variables in the domain of the expression. The SOP expression AC + BC is not a standard SOP as the domain of the expression has variables A, B and C.

A non-standard SOP is converted into a standard SOP by using the rule $A + \bar{A} = 1$

Standard POS form

A standard POS form has sum terms that have all the variables in the domain of the expression. The POS expression (A + B + C)(A + B + D)(A + B + C + D) is not a standard POS as the domain of the expression has variables A, B, C and D.

A non-standard POS is converted into a standard POS by using the rule $A\bar{A} = 0$

Converting to Standard SOP and POS forms

There are several reasons for converting SOP and POS forms into standard SOP and POS forms respectively.

Any logic circuit can be implemented by using either the SOP, AND-OR combination of gates or POS, OR-AND combination of gates. It is very simple to convert from standard SOP to standard POS or vice versa. This helps in selecting an implementation that requires the minimum number of gates. Secondly, the simplification of general Boolean expression by applying the laws, rules and theorems does not always result in the simplest form as the ability to apply all the rules depends on one's experience and knowledge of all the rules.

A simpler mapping method uses Karnaugh maps to simplify general expressions. Mapping of all the terms in a SOP form expression and the sum terms in a POS form can be easily done if standard forms of SOP and POS expressions are used.

Lastly, the PLDs are implemented having a general purpose structure based on ANDOR arrays. A function represented by an expression in Standard SOP form can be readily programmed.

Minterms and Maxterms: The Product terms in the Standard SOP form are known as Minterms and the Sum terms in the Standard POS form are known as Maxterms.

Binary representation of a standard Product term or Minterm: A standard product term is equal to one for only one combination of variable values. For all other variable values the standard product term is equal to zero.

Converting Standard SOP into Standard POS: The binary values of the product terms in a given standard SOP expression are not present in the equivalent standard POS expression. Also, the binary values that are not represented in the SOP expression are present in the equivalent POS expression.

Boolean Expressions and Truth Tables: All standard Boolean expressions can be easily converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Converting SOP expression to Truth Table format: A truth table is a list of possible input variable combinations and their corresponding output values. An SOP expression having a domain of 2 variables will have a truth table having 4 combinations of inputs and corresponding output values. To convert an SOP expression in a Truth table format, a truth table having input combinations proportional to the domain of variables in the SOP expression is written. Next the SOP expression is written in a standard SOP form. In the last step all the sum terms present in the standard SOP expression are marked as 1 in the output.

Converting POS expression to Truth Table format: An POS expression having a domain of 2 variables will have a truth table having 4 combinations of inputs and corresponding output values. To convert a POS expression in a Truth table format, a truth table having input combinations proportional to the domain of variables in the POS expression is written. Next the POS expression is written in a standard POS form. In the last step all the product terms present in the standard POS expression are marked as 0 in the output.

$(A + \bar{B})(B + \bar{C})$ has a domain of three variables thus a truth table having 8 input and output combinations is required. The POS expression is converted into standard POS expression.

Lecture No 10

KARNAUGH MAP & BOOLEAN EXPRESSION SIMPLIFICATION

Simplifying Boolean Expressions using the laws, rules and theorems do not guarantee the simplest form of expression as sometimes simplification of certain terms is not so obvious or the person doesn't have the necessary experience in applying the laws and rules. The Karnaugh Map provides a systematic method for simplifying Boolean expressions. A Karnaugh Map is organized in the form of an array. Adjacent cells of the array can be grouped together to result in simplification of a given expression. Karnaugh Maps can be used to simplify expressions of 2, 3, 4 and 5 variables.

The 3-variable Karnaugh Map:

AB\C	**0**	**1**
00	**0**	**1**
01	**2**	**3**
11	**6**	**7**
10	**4**	**5**

A\BC	**00**	**01**	**11**	**10**
0	**0**	**1**	**3**	**2**
1	**4**	**5**	**7**	**6**

• A 3-variable K-Map has an array of 8 cells. The 8 cells can be arranged in 2 columns and 4 rows representing the column form of the Karnaugh Map.
• Alternately, the 8 cells can be organized in 2 rows and 4 columns representing the row form of the Karnaugh map.
• Any of the two forms of the Karnaugh Map can be used to simplify Boolean expressions. The simplified expressions using either of the two K-maps are identical.
• Considering first the column based 3-variable Karnuagh map. The binary values 00, 01, 11 and 10 in the left most column of the K-map represent the binary values of variables A and B. The binary values 0 and 1 in the top row of the K-map represent the binary values of variable C.
• The 3-variable K-Map based on the row representation is considered next. The binary values 0 and 1 in the left most column of the K-map represent the binary values of variable A. The binary values 00, 01, 11 and 10 in the top row of the K-map represent the binary values of variables B and C
• The numbers in the cells represent the Minterms or Maxterms of an expression that is to be represented using the K-map. The cell marked 0 for example, represents the minterm 0 or the maxterm 0 having binary value of variables A, B and C equal to 000. Similarly cell marked 5 represents the minterm 5 or the maxterm 5 having binary values of variables A, B and C equal to 101.

Grouping and Adjacent Cells: Karnaugh Map Array is considered to be wrapped around were all sides are adjacent to each other. Groups of 2, 4, 8, 16, 32 etc. adjacent cells are formed. Adjacent cells can be
• row wise • column wise • four corner cells • row-column groups of 4, 8, 16, 32 etc
Groups are formed on the basis of 1s (Minterms) or 0s (maxterms). A group is selected to have maximum number of cells of Minterms or Maxterms, keeping in view that the size of the group should be a power of 2. The idea is to form minimal number of largest groups that uniquely cover all the cells, thereby ensuring that all minterms or maxterms are included.

Mapping a standard SOP Expression: The first step in simplification of Boolean expressions is to map the expressions to the Karnaugh maps. For a Standard SOP expression, a 1 is placed in the cell corresponding to the product term (Minterm) present in the expression. The cells that are not filled with 1s have 0s. The Standard SOP expression having a Domain of three variables $AB\bar{C} + A\overline{BC} + \bar{A}B\bar{C}$ is mapped to a 3-Variable Karnaugh Map. The product terms or the Minterms are 2, 4 and 6. The expression is mapped on a K-Map by placing a 1 at Minterm cells 2, 4 and 6 and placing 0 at remaining cells.

Mapping a non-standard SOP Expression: In many practical cases, SOP expressions are not in a standard format. To map them to K-maps they have to be either converted into Standard SOP expressions or they can be directly mapped.

Example 1: The expression $A + B\bar{C}$ is a non-standard SOP expression having a domain of 3 variables. If the expression is converted into a standard SOP expression then there will be four product terms having the variable A. Similarly, there would be two product terms having the variable combination $B\bar{C}$. Two of the product terms $AB\bar{C}$ are identical. The expression $A + B\bar{C}$ can be directly mapped to a K-map without first converting the expression to the standard form.

AB\C	0	1
00	0	0
01	1	0

11	1	1
10	1	1

The term A is mapped first. A '1' is marked in cells where the variable A is present.

A\BC	00	01	11	10
0				
1	**1**	**1**	**1**	**1**

Simplification of SOP expressions using the Karnaugh Map

SOP expressions can be very easily simplified using the K-Map method. In the first step of the simplification process, the SOP expression is mapped on the K-map. In the next step, groups of 1s are formed starting with the largest group of 1s. The group should be of size 2, 4, 8, 16 etc. having adjacent 1s. Multiple (unique) groups of 1s are formed. All the groups formed can either be separate groups or they could share common 1s each having at least a single 1 that is not common to any other group. A single 1 that is not adjacent to any other 1 is considered as a group having only a single cell.

A 3-variable K-map yields

- A product term of three variables for a group of 1 cell
- A product term of two variables for a group of 2 cell
- A product term of one variable for a group of 4 cell
- A group of 8 cells yields a value of 1 for the expression.

A 4-variable K-map yields

- A product term of four variables for a group of 1 cell
- A product term of three variables for a group of 2 cell
- A product term of two variables for a group of 4 cell
- A product term of one variable for a group of 8 cell
- A group of 16 cells yields a value of 1 for the expression.

Mapping Directly from Function Table

Practically, when a digital circuit is to be implemented to perform some operation, its function is first defined using a function table. The information in the function table is directly mapped to a K-map of appropriate variables which is then simplified. The simplified expression obtained from the K-map is directly implemented using logic Gates.

Don't care Conditions: Don't care conditions are marked as x in the output column of the function table corresponding to the don't care conditions. When the function table is mapped to the process for simplification of the SOP expression the x outputs can be considered as 0 or 1. By assigning a 0 or 1 to the cells marked with x, the final expression can be significantly simplified.

Lecture No 11

Mapping a Standard POS Expression For a Standard POS expression, a 0 is placed in the cell corresponding to the product term (maxterm) present in the expression. The cells are not filled with 0s have 1s. The Standard POS expression having a Domain of three variables

$(A + B + \bar{C}).(A + \bar{B} + C).(\bar{A} + B + \bar{C}).(\bar{A} + \bar{B} + \bar{C})$ uses a 3-Variable Karnaugh Map. The sum terms or the Maxterms are 1, 2, 5 and 7. The expression can be represented by a K-Map by placing a 0 at Maxterm locations 1, 2, 5 and 7 and placing 1 at remaining places. Any of the two K-maps can be used.

AB\C	0	1
00	1	0
01	0	1
11	1	0
10	1	0

A\BC	00	0	11	10
0	1	0	1	0
1	1	0	0	1

Karnaugh Map simplification of POS expressions: POS expressions can be easily simplified by use of the K-Map in a manner similar to the method adopted for simplifying SOP expressions. After the POS expression is mapped on the K-map, groups of 0s are marked instead of 1s based on the rules for forming groups used for simplifying SOP. In the next

step minimal sum terms are determined. Each group, including a group having a single cell, represents a sum term having variables that occur in only one form either complemented or un-complemented.

Converting between POS and SOP using the K-map: Converting between the two forms of standard expressions is very simple. If the 1s mapped on the K-map are grouped together they form the product terms of the SOP expression. Similarly, if the 0s mapped on the K-map are grouped together they form the sum terms of the POS expression

7-Segment Display: The 7-segment display digit is shown. Figure 11.10. 7-Segment Display is used to display the decimal numbers 0 to 9. A 7-segment display digit has 7 segments a, b, c, d, e, f and g that are turned on/off by a digital circuit depending upon the number that is to be displayed.

Digit	Segments
0	**A, b, c, d, e, f**
1	b, c
2	a, b, d, e, g
3	a, b, c, d, g
4	b, c, f, g
5	a, c , d, f, g
6	a, c, d, e, f, g
7	a, b, c
8	a, b, c, d, e, f, g
9	a, b, c, d, f, g

Lecture No 12

COMPARATOR: A comparator circuit compares two numbers and sets one of its three outputs to 1 indicating the result of the comparison operation. A Comparator circuit has multiple inputs and three outputs.

A 2-bit Comparator circuit compares two 2-bit numbers A and B. The comparator circuit has three outputs. It sets the A>B output to 1 if A>B. It sets the A=B output to 1 if A=B and sets A<B output to 1 if A < B.

• The output A>B is set to 1 when the input combinations are 01 00, 10 00, 10 01, 11 00, 11 01 and 11 10

• The output A=B is set to 1 when the input combinations are 00 00, 01 01, 10 10 and 11 11

• The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

The circuit has 4-bit input, 2-bits represent A and 2-bits represent B and a 3-bit output representing A>B, A=B and A<B. To represent the function of a Comparator circuit, three function tables are required for each of the three outputs. A single function table is drawn with three outputs.

Each of the three outputs, A>B, A=B and A<B are mapped separately using three 4- variable Karnaugh maps.

Quine-McCluskey Simplification Method: Karnuagh map method becomes difficult to manage when numbers of variables exceed 4. Even with a 4-varaiable K-map, grouping of 1s or 0s depends on the ability of the user to detect optimum groups. Sometimes some redundant groups are included which adds a product term or a sum term which is not required and thus the expression is not the simplified version.

Quine-McCluskey is a program based method that is able to carry out the exhaustive search for removing shared variables. The Quine-McCluskey method is a two-step method which comprises of finding Prime Implicants and selecting a minimal set of Prime Implicants.

• Find Prime Implicants: Find by an exhaustive search all the terms that are candidates for inclusion in the simplified function. These terms are known as Prime Implicants.

• Selecting Minimal Set of Prime Implicants: Choose from amongst the Prime Implicants those that give expression with the least number of literals.

Comparator Circuit: A 2-bit Comparator circuit that compares two 2-bit numbers A and B and activates one of its three outputs A>B, A=B and A<B depending upon the magnitudes of the numbers A and B has been discussed earlier. The function outputs of the three outputs A>B, A=B and A<B can easily be represented using truth tables which can then be written in a simplified Boolean expression form after simplifying the three function expressions using 4-variable Karnaugh maps.

A comparator circuit that compares two 3-bit numbers A and B instead of the 2-bit numbers has an input of 6-bits, which represents an input combination of 64. Writing a truth table and simplifying the three expressions using the 6-variable Karnaugh maps becomes unmanageable. A program based Quine-McCluskey method can easily handle expression of 6 variables represented in the Canonical form $(8,16,17,24,.....)_{A,B,C,D,E,F}\Sigma$

Odd-Prime Number Detector

A circuit that detects Odd Prime numbers between 0 and 9 has been considered earlier. The circuit is to be improved to detect Odd Prime numbers for a decimal number rangerepresented by 5-bit binary numbers or in terms of decimal numbers between the decimal numbers ranges 0 to 31. Writing out a function table to represent the 32 input combinations and their corresponding outputs, and then simplifying the function expression using a 5-varaibale

K-map can take up considerable amount of time.

Quine-McCluskey method can be used to easily simplify the 5-variable Boolean expression represented in Canonical Sum form as $(1,3,5,7,11,13,17,19,23,29,31)_{A,B,C,D,E}\Sigma$. The minterms 1, 3, 5, 7, 11, 13, 17, 19, 23, 29 and 31 represent the 5-bit input combinations (decimal numbers) which are Odd and Prime numbers.

Lecture No 13

Combinational Logic: Individual gates AND, OR and NOT, NAND and NOR Universal Gates and XOR and XNOR gates perform unique functions. These gates in their individual capacity can not perform any useful function. The Logic Gates have to be connected together in different combinations to form Logic Circuits that are able to perform some useful operation like addition , comparison etc. These combinations of gates which results in a circuit used to perform some function are known as Combinational Logic.

The function of any Digital Logic circuit is represented by Boolean expressions. In the examples discussed earlier, Boolean expressions for various functions have been determined. Two forms of representing functions through Boolean expressions are the SOP and POS expressions. These two types of Boolean expressions are implemented using a combination of gates to form Combinational Logic Circuits.

Combinational Circuit Implementation based on SOP form: A standard way to express a Boolean expression is the SOP form. The expression has several product terms which are summed together through a single OR gate. The product terms can have variables and their complemented form. A SOP expression is implemented by using a combinational circuit made up of many AND gates and a single OR gate (AND-OR gate combination). The inputs to the AND gates can be in the complemented form or the un-complemented form, requiring the use of NOT gates.

Combinational Circuit Implementation based on POS form

A standard way to express a Boolean expression is the POS form. The expression has several sum terms which are multiplied together through a single AND gate. The sum terms can have variables and their complemented form. A POS expression is implemented by using a combinational circuit made up of many OR gates and a single AND gate (OR-AND gate combination). The inputs to the OR gates can be in the complemented form or the un-complemented form, requiring the use of NOT gates.

Design and Implementation of Combinational Circuits

The design and implementation of a combinational circuit starts by defining the function of the Combinational circuit. The function of a combinational circuit is defined by a truth table or a function table. Once the function table is defined the combinational circuit can be directly implemented from the function table.

Direct implementation of a combinational circuit from the function table results in a circuit which uses maximum number of gates organized at three levels. This increases the cost, the size of the circuit and the power requirement of the Combinational circuit. The propagation delay of the circuit is of the order of three gates. Therefore, before implementing the circuit the expression is simplified using the manual method by applying rules, laws and theorems of Boolean Algebra or by the Karnaugh map method or the Quine-McCluskey method if the number of variables exceeds 4.

Implementation of an Adjacent 1s Detector Circuit

A circuit that checks an input number and determines if it has two adjacent 1s is considered to explain the entire process of design and implementation of a typical Combinational Logic Circuit. The Adjacent 1s detector circuit is implemented using the standard SOP and POS forms of Boolean expressions. The circuit is also implemented using the simplified Boolean expressions. The alternate form of implementing the circuit using only NAND or NOR gates is also discussed.

Operation of Adjacent 1s detector Circuit

The operation of a Combinational Logic Circuit can be verified by applying varying set of signals at the input of the circuit and comparing the output of the combinational circuit with the corresponding outputs in the Function Table. If the varying set of inputs and the corresponding outputs are plotted over a period of time, the timing diagram thus obtained, describes the operation of the circuit.

Active low/high Inputs and Outputs

The circuits discussed so far have their output set to when to indicate an active state. For example, the output of the BCD to 7-Segment Decoder circuit has its seven segment outputs set to 1 to indicate a segment that has been selected. Similarly, the Comparator circuit's three outputs are normally at binary 0. The appropriate output is set to 1 to indicate the relationship between the two numbers. The Odd-Prime Number detector circuit output normally is set at 0. It is activated to 1 to indicate an Odd-Prime number. The Adjacent 1s

Detector circuit also sets its output to active 1 to indicate detection of Adjacent 1s. All the four circuits have an active-high output. That is, normally the output is at logic 0. The output is set to 1 to indicate an active state.

Combinational circuits can have an active-high output or an active-low output. An active-high or active-low output doesn't effect the operation of the combinational circuit in any manner. To convert a circuit having an active-high output to active low-output requires the inversion of the circuit output by connecting a NOT gate. Symbolically, a bubble is added to the circuit output. Thus, circuits having a bubble at their outputs are considered to have an active-low output.

Lecture No 14

IMPLEMENTATION OF AN ODD-PARITY GENERATOR CIRCUIT

The first step in implementing any circuit is to represent its operation in terms of a Truth or Function table. The function table for an 8-bit data as input has 2_8 has 256 input combinations, which becomes unmanageable. Therefore, for the sake of simplicity a 4-bit data with odd parity is assumed. The receiver circuit is also based on the 4-bit data.

XOR and XNOR Gates

XOR and XNOR gates are used to implement the Odd-Parity Generator Circuit. An XNOR is also used to check for single bit errors at the Receiver end. Both, the XOR and XNOR gates perform simple comparison functions. The XOR gate detects dissimilar inputs, where as the XNOR gate looks for similar inputs. Both, the gates can be considered as functional devices as each gate performs a simple specific function. The XOR and XNOR gates are implemented using a combination of NOT, AND and OR gates. Since the function performed by the XOR and XNOR gate is commonly used in digital circuits therefore XOR and XNOR gates are available in Integrated circuit form which can be readily used instead of implementing an XOR and XNOR circuit based on NOT-ANDOR combination of gates.

Combinational Function Devices

Digital circuits are formed by the combination of Logic Gates. Most Combinationalcircuits perform standard and useful functions such as addition, comparison, decoding and encoding, multiplexing and de-multiplexing, selection and enabling of devices and many more operations. Implementation of these standard functional devices through combination of gates takes up considerable space, therefore these functional devices are implemented as MSI or Medium Scale Integrated Chips.

The simplest of these functional devices can be considered to be the NAND and NOR gates which perform the AND-NOT and OR-NOT functions. The XOR and XNOR Gates are also a combination of NOT-AND-OR gates which perform functions to detect dissimilar and similar inputs.

Half Adder and Full Adder

A single bit binary adder circuit basically adds two bits and a carry bit, generated by the addition of the least significant bits. The output of the single bit adder circuit generates a sum bit and a carry bit. A single digit binary adder circuit therefore has three inputs, one representing single bit number A, the other representing the single bit number B and the third bit represents the single bit carry. The single bit binary adder has two bit output. One bit represents the Sum between numbers A and B. The other bit represents the carry bit generated due to addition. In Digital logic terminology the adder which has been described is known as a full adder. An adder circuit that only has two bit input representing the two single bit numbers A and B and does not have the carry bit input from the least significant digit is regarded as a half-adder. The block diagrams represent a Half-Adder and a Full-Adder.

1. Half-Adder

A Half-Adder can be fully described in terms of its Function table, its Sum and Carry Out Boolean Expressions and the circuit Implementation.

Half-Adder Function Table

The Half-Adder has a 2-bit input and a 2-bit output. The function table of the Half-Adder has two input columns representing the two single bit numbers A and B. The function table also has two output columns representing the Sum bit and Carry Out bit.

2. Full-Adder

A Full-Adder can be fully described in terms of its Function table, its Sum and Carry Out Boolean Expressions and the circuit Implementation.

Full-Adder Function Table

The Full-Adder has a 3-bit input and a 2-bit output. The function table of the Full-Adder has three input columns representing the two single bit numbers A, B and the Carry In bit. The function table also has two output columns representing the Sum bit and Carry Out bit.

Forming a Full-Adder using Half-Adders

A 1-bit Full-Adder cane be implemented by combining together two Half-Adders.

Parallel Binary Adders

Single bit Full or Half Adders do not perform any useful function. To add two 4-bit numbers a 4-bit adder is required. Four single bit Full-Adders are connected together to form a 4-bit Parallel Adder capable of adding two 4-bit binary numbers.

MSI Adders

4-bit parallel Adders are available as Medium Scale Integrated Circuits. These circuits use the Look-Ahead Carry Circuitry to remove the carry ripple. The two ICS are 74LS83A and 74LS283. Both the devices are functionally identical, however they are not pin compatible.

These devices are packaged as 16-pin devices. The division of the 16 pins is

• 4 pins for the 4-bit input A • 4 pins for the 4-bit input B • 4 pins for the 4-bit output Sum
• 1 pin for Carry In • 1 pin for Carry Out • 1 pin for Circuit Power Supply • 1 pin for Circuit GND

Lecture No 15

BCD ADDER: BCD binary numbers represent Decimal digits 0 to 9. A 4-bit BCD code is used to represent the ten numbers 0 to 9. Since the 4-bit Code allows 16 possibilities, therefore the first 10 4-bit combinations are considered to be valid BCD combinations. The latter six combinations are invalid and do not occur.

BCD Code has applications in Decimal Number display Systems such as Counters and Digital Clocks. BCD Numbers can be added together using BCD Addition. BCD Addition is similar to normal Binary Addition except for the case when sum of two BCD digits exceeds 9 or a Carry is generated. When the Sum of two BCD numbers exceeds 9 or a Carry is generated a 6 is added to convert the invalid number into a valid number. The carry generated by adding a 6 to the invalid BDC digit is passed on to the next BCD digit.

Addition of two BCD digits requires two 4-bit Parallel Adder Circuits. One 4-bit Parallel Adder adds the two BCD digits. A BCD Adder uses a circuit which checks the result at the output of the first adder circuit to determine if the result has exceeded 9 or a Carry has been generated. If the circuit determines any of the two error conditions the circuit adds a 6 to the original result using the second Adder circuit. The output of the second Adder gives the correct BCD output. If the circuit finds the result of the first Adder circuit to be a valid BCD number (between 0 and 9 and no Carry has been generated), the circuit adds a zero to the valid BCD result using the second Adder. The output of the second Adder gives the same result.

Connection of Invalid BCD Detector Circuit to second Adder

Adding of 6 when error conditions are detected and adding a zero when error conditions are not detected is implemented by connecting the output of the Invalid BCD Number Detector circuit to bits B_1 and B_2 of the Adder. Bits B_0 and B_3 are permanently connected to 0.

2-digit BCD Adder

Two singe digit BCD Adders can be cascaded together to form a 2-digit BCD Adder. Four, 4-bit 74LS283 MSI chips are used. Two 74LS283s are required to directly add the two 2- digit BCD numbers and the remaining two 74LS283s are required to add a six to the result if any of the two digits add up to invalid BCD digits or generate a Carry. Two invalid BCD detector circuits are used.

Subtraction: Subtraction in Digital Systems is performed by taking the 2's complement of the number to be subtracted (subtrahend) and adding it to the minuend. The example shows the subtraction of 6 represented in 2's complement form from nine also represented in its 2's complement form. Since 9 is a positive number therefore its 2's complement representation is the same. Neglecting the carry bit, the 4-bit number represents decimal 4.

```
 9      1001
-5      1011
4    1 0100
```

Arithmetic and Logic Unit (ALU)

Microprocessors have Arithmetic and Logic Units, a combinational circuit that can perform any of the arithmetic operations and logic operations on two input values. The operation to be performed is selected by set of inputs known as function select inputs.

There are different MSI ALUs available that have two 4-bit inputs a 4-bit output and three to five function select inputs that allows up to 32 different functions to be performed.

Three commercially available 4-bit ALUS are

• 74XX181: The 4-bit ALU has five function select inputs allowing it to perform 32 different Arithmetic and Logic operations.

• 74XX381: The 4-bit ALU only has three function select inputs allowing only 8 different arithmetic and logic functions. Table 15.6

• 74XX382: The 4-bit ALU is similar to the 74XX381, the only difference is that 74XX 381 provides group-carry look-ahead outputs and 74XX382 provides ripple carry and overflow outputs

Implementing 16-bit ALU

16-bit ALU can be implemented by cascading together four 4-bit ALUs. These 4-bit ALUs have built in Look-Ahead Carry Generator circuits that eliminate the delay caused by carry bit propagating through the Parallel Adder circuit within the 4-bit ALU circut. However, when a number of such units are cascaded together to implement large 16-bit and 32-bit ALU, the carry propagating between one unit to the next gets delayed due to the Carry rippling through multiple 4-bit units. For large 32-bit ALUs, the Carry propagates through 8, 4-bit units delaying the Carry out from the last most significant unit by a factor of 8.The 74XX181 and 74XX381 circumvent the problem by having Group-Carry Look-Ahead.

Lecture No 16

Comparators: The basic function of a Comparator is to compare two binary quantities and to determine if the two quantities are equal. If the quantities are not equal then it has to determine which of the two quantities is greater than the other. Many Integrated Circuit Comparators have three outputs to indicate A=B, A>B and A<B.

Earlier, simplified Boolean expressions for a 2-bit Comparator circuit were determined that compares two 2-bit numbers and sets one of its three outputs to indicate A=B, A>B or A<B. The Booleans expressions representing the three outputs are presented.

The 2-bit Comparator discussed earlier is considered to be a Parallel Comparator as all the bits are compared simultaneously. External Logic has to be used to Cascade together two such Comparators to form a 4-bit Comparator.

The two most significant bits of 4-bit numbers A and B are compared by the Most Significant 2-bit Comparator M and the least significant two bits are compared by the Least Significant 2-bit Comparator L.

Iterative Circuit based Comparator: An Iterative circuit is implemented using identical modules each of which has Primary Inputs and Outputs and Cascading Inputs and Outputs. The Cascading inputs of the least significant module are connected to fixed logic inputs and the Cascading outputs are connected to the Cascading inputs of the next significant module.

MSI 4-bit Comparator: MSI 74HC85 4-bit Iterative Circuit based Comparator allows multiple 74HC85s to be cascaded together to form Comparators N x 4-bit Comparators. Three 74HC85s cascaded together forms a 12-bit Comparator circuit.

Decoders: A Decoder has multiple inputs and multiple outputs. The Decoder device accepts as an input a multi-bit code and activates one or more of its outputs to indicate the presence of the multi-bit code. There are different variations of Decoder devices.

Basic Decoder: Consider an electronic door lock which unlocks the door when a 4-bit code 1011 is entered. The door is locked when another 4-bit combination 1001 is entered. The lock and unlock circuit is implemented using a combination of NOT and AND gates.

Applications of decoders: Decoders have two major uses in Computer Systems.

1. Selection of Peripheral Devices: Computers have different internal and external devices like the Hard Disk, CD Drive, Modem, Printer etc. Each of these different devices is selected by specifying different codes. A decoder similar to the Electronic Door Lock/Unlock circuit is used to uniquely select or deselect the appropriate devices.

2. Instruction Decoder: Computer programs are based on instructions which are decode by the Computer Hardware and implemented. The codes 1100010, 1100011, 1110000 and 1000101 represent Add two numbers, Subtract two numbers, Clear the result and Store the result instructions. These instruction codes are decoded by an Instruction Decoder to generate signals that control different logic circuits like the ALU and memory to perform these operations.

Binary Decoder: The simplest and most commonly used Decoders are the n-to-2_n Decoders. These Decoders have n inputs and 2_n outputs Each, n-bit input selects 1 out of 2_n output code. A 2-to-4 Decoder is represented by the function table. Table16.2.

MSI Decoder: The 74LS139 MSI chip has dual 2-to-4 Decoders.

Lecture No 17

THE 74XX138 3-TO-8 DECODER:

The 3-to-8, 74XX138 Decoder is also commonly used in logical circuits. Similar, to the 2-to-4 Decoder, the 3-to-8 Decoder has active-low outputs and three extra NOT gates connected at the three inputs to reduce the four unit load to a single unit load. The 3-to-8 Decoder has three enable inputs, one of the three enable inputs is active-high and the remaining two are active-low. All three enable inputs have to be activated for the Decoder to work.

The three enable inputs serve to implement to larger Decoders such as 4-to-16 and 5-to-32 by cascading two or four 3-to-8 Decoders respectively.

BCD to 7-Segment Decoder

BCD to 7-Segmnet Decoder is a specific type of decoder that is used to convert a 4-bit BCD Code to a 7-Segment Code. The BCD to 7-Segment Decoder unlike the Binary Decoders activates multiple but unique set of outputs for each 4-bit BCD input combination. Earlier, the seven expressions for activating each of the seven segments were defined. Each of the seven Boolean expressions can be implemented using a combination of NOTAND- OR gates.

MSI Seven-Segment Decoder

The 7-Segment Decoder circuit is available in MSI form, 74LS47. The IC has 4-bit BCD input ABCD and 7-bit active-low outputs for segments a, b, c, d, e, f and g. The Decoder also has three extra active-low inputs.

- LT: Lamp test
- RBI: Ripple Blanking Input
- BI/RBO: Blanking Input/Ripple Blanking Output

When a low is applied to the LT input and the BI/RBO is high, all of the seven segments in the display are turned on to test that no segments are burned out. The Ripple Blanking Input and The Blanking Input/Ripple Blanking Outputs are used to prevent display of leading and trailing zeros.

BCD-to-Decimal Decoder

The operation of the BCD-to-Decimal Decoder is the same as a Binary 4-to-16 decoder, the only difference being that the BCD-to-Decimal Decoder has ten output pins instead of sixteen and the input is a valid BCD number. Thus invalid BCD codes 1010, 1011, 1100, 1101, 1110 and 1111 applied at the input of the Decoder do not activate any of the ten outputs. The commercially available MSI, BCD-to-Decimal Decoder is the 74LS42, which has active-high inputs and active-low outputs.

Encoder

An Encoder functional device performs an operation which is the opposite of the Decoder function. The Encoder accepts an active level at one of its inputs and at its output generates a BCD or Binary output representing the selected input. There are various types of Encoders that are used in Combinational Logic Circuits.

Binary Encoder

The simplest of the Encoders are the 2_n-to-n Encoders. The functional table and the circuit diagram of an 8-to-3 Binary Encoder are shown in table 17.2 and figure 17.6 respectively.

Priority Encoders

Priority Encoders remove the problem highlighted earlier with simple Binary Encoders. Priority Encoders have necessary logic to activate the outputs corresponding to the highest Priority input when multiple inputs are asserted simultaneously.

Cascading Priority Encoders

The 74XX148 Priority Encoder has active-low inputs and active-low outputs. The Encoder also has an active-low enable input E1 which enables or disables the outputs. The
Group Select GS active-low output is asserted when any one of the inputs is asserted. The Enable output EO signal is used to cascade multiple Encoders to form larger Encoders. The EO output is connected to the EI input of the Encoder which handles lower priority inputs. Two 8-input are shown connected together to form a 16-input Priority Encoder.

Decimal-to-BCD Encoder

The Decimal-to-BCD Encoder has ten inputs, for the decimal digits 0 to 9 and four outputs corresponding to the 4-bit BCD output. The 74LS147 is a Decimal-to-BCD Priority Encoder which has active-low input and outputs. The Decimal-to-BCD Priority Encoder is used as a keypad encoder. A telephone keypad has digits 0 to 9. The keypad is connected to the encoder through pull-up resistors that ensure that the inputs to the encoder are logic high when none of the keypad keys is pressed. Whenever a key is pressed the appropriate input of the encoder is connected to logic low and at the output the corresponding BCD code is generated.

Multiplexer

Multiplexer is a digital switch that has several inputs and a single output. The Multiplexer also has select inputs that allow any one of the multiple inputs can be selected to be connected to the output. Multiplexers are also known as Data Selectors. The main use of the Multiplexer is to select data from multiple sources and to route it to a single Destination. In a computer, the ALU combinational circuit has two inputs to allow arithmetic operations to be performed on two quantities. The two quantities are usually stored in different set of registers. The inputs of the two multiplexers are connected to the output of each of the multiple registers. The outputs of the two multiplexers are connected to the two inputs of the ALUs. The Multiplexers are used to route the contents of any two registers to the ALU inputs.

Dual 4-Input Multiplexer

Commercial available 4-input Multiplexer is the 74XX153 IC which has two 4-input multiplexers. The two select inputs of the two 4-input multiplexers are common, however each multiplexer has a separate enable input which allows the two multiplexers to be separately controlled.

Lecture No 18

2-INPUT 4-BIT MULTIPLEXER

The MSI, 74X157 is a 2-input, 4-bit Multiplexer. This multiplexer has two sets of 4-bit inputs. It also has 4-bit outputs. The single select input line allows the first set of four inputs or the second set of 4-inputs to be connected to the output. Thus four-bits of data from two sources are routed to the output.

Expanding Multiplexers

Multiplexers have to be connected together to form larger multiplexer to fulfil specific application requirements.

8-Input Mutliplexer

A single dual, 4-input multiplexer 74X153 can be connected to form an 8-input multiplexer.

16-Input Multiplexer

Two 74XX153 Dual, 4-input multiplexer can be connected to form a 16-input multiplexer.

2-Input, 8-bit Multiplexer

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a 2-input, 8-bit multiplexer.

Applications of Multiplexers

Multiplexers are used in a wide variety of applications. Their primary use is to route data from multiple sources to a single destination. Other than its use as a Data router, a parallel to serial converter, logic function generator and used for operation sequencing.

1. Data Routnig

A two digit 7-Segment display uses two 7-Segments Display digits connected to two BCD to 7-Segment display circuits. To display the number 29 the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-Segment display circuit connected to the MSD 7-Segment Display Digit. Similarly, the BCD input 1001 representing the numbers 9 is applied at the inputs of the LSD display circuit. The circuit uses two BCD to 7-Segment decoder circuits to decode each of the two BCD inputs to the respective 7- Segment display outputs.

Common Anode 7-Segment Display

The Common Anode 7-Segment Display has positive end of each of the seven display segments (LEDs) connected together. To display any segment the Common Anode of the display has to be connected to +5 volts and the other end of each segment has to be connected to 0 volts.

Common Cathode 7-Segment Display

The Common Cathode 7-Segment Display has negative end of each of the seven display segments (LEDs) connected together. To display any segment the Common Cathode of the display has to be connected to 0 volts and the other end of each segment has to be connected to +5 volts.

2. Parallel to Series Conversion

In a Digital System, Binary data is used and represented in parallel. Parallel data is a set of multiple bits. For example, a nibble is a parallel set of 4-bits, a byte is a parallel set of 8 bits. When two binary numbers are added, the two numbers are represented in parallel and the parallel adder works and generates a sum term which is also in parallel.

Transmission of information to remote locations through a piece of wire requires that the parallel information (data) be converted into serial form. In a serial data representation, data is represented by a sequence of single bits. An 8-bit parallel data can be transmitted through a single piece of wire 1-bit at a time. Transmitting 8-bits simultaneously (in parallel form) requires 8 separate wires for the 8-bits. Laying of 8 wires across two remote locations for data transfer is expensive and is therefore not practical. All communication systems set up across remote locations use serial transmission.

An 8-bit parallel data can be converted into serial data by using an 8-to-1 multiplexer such as 74X151 which has 8 inputs and a single output. The 8-bit data which is to be transmitted serially is applied at the 8 inputs $I_{0\text{-}7}$ of the multiplexer.

3. Logic Function Generator

Multiplexers can be used to implement a logic function directly from the function table without the need for simplification. The select inputs of the multiplexer are used as the function variables. The inputs of the multiplexer are connected to logic 1 and 0 to represent the missing and available terms.

4. Operation Sequencing

Many industrial applications have processes that run in a sequence. A paint manufacturing plant might have a four step process to manufacture paint. Each of the four steps runs in a sequence one after the other. The second step can not start before the first step has completed. Similarly, the third and fourth step of the paint manufacturing process can not proceed unless steps two and three have completed. It is not necessary that each of the manufacturing steps is of the same duration. Each manufacturing step can have different time duration and can be variable depending upon the quantity of paint manufactured or other parameters. Normally, the end of each step in the manufacturing process is indicated by a signal which is actuated by some machine which has completed its part of the manufacturing process. On receiving the signal the next step of the manufacturing process is initiated.

Lecture No 19

DEMULTIPLEXER

A Multiplexer has several inputs. It selects one of the inputs and routes the data at the selected input to the single output. Demultiplexer has an opposite function to that of the Multiplexer. It has a single input and several outputs. The Demultiplexer selects one of the several outputs and routes the data at the single input to the selected output. A demultiplexer is also known as a Data Distributor.

Applications of Demultiplexer

Demultiplexer is used to connect a single source to multiple destinations. One use of the Demultiplexer is at the output of the ALU circuit. The output of the ALU has to be stored in one of the multiple registers or storage units. The Data input of the Demultiplexer is connected to the output of the ALU. Each output of the Demultiplexer is connected to each of the multiple registers. By selecting the appropriate output data from the ALU is routed to the appropriate register for storage.

The second use of the Demultiplexer is the reconstruction of Parallel Data from the incoming serial data stream. Serial data arrives at the Data input of the Demultiplexer at fixed time intervals. A counter attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored. When all the bits have been stored, data can be read out in parallel.

Programmable Logic Devices

Programmable Logic Devices are used in many applications to replace the Logic gates and MSI chips. PLDs save circuit space and reduce and save the cost of components in a Digital Circuit. PLDS consists of Arrays of AND gates and OR gates that can be programmed to perform specific functions.

Programmable Arrays of AND Gates and OR Gates

The array is essentially a grid of conductors that forms rows and columns with a fuse connecting each column conductor with each row conductor. The fuses can be blown to disconnect a particular column from a particular row. The OR gate array consists of the grid and OR gates. Similarly the AND gate array consists of the grid and AND Gates.

1. Programmable Read-Only Memory (PROM)

The PROM consists of a fixed non-programmable AND array configured as a decoder and a programmable OR array. The PROM is used as a storage device which stores information at addressable locations. It has limited applications and is not used as a logic device.

2. Programmable Logic Array (PLA)

The PLA consists of a programmable AND array and a programmable OR array. It has been designed to overcome the limitations of a PROM. PLA is also known as a Field-Programmable Logic Array as it can be programmed by the user and not by the manufacturer.

3. Programmable Array Logic (PAL)

The PAL has been designed to overcome the longer delays and the complex circuitry associated with the PLA due to two programmable arrays. The PAL has programmable AND array and a fixed OR array.

4. Generic Array Logic (GAL)

The GAL has a reprogrammable AND array and a fixed OR array with programmable output logic.The main difference between GAL and PAL are the reprogrammable AND array which can be programmed again and again, unlike PAL AND array which can be programmed once. GAL uses E^2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links. The other difference is the programmable outputs.

PAL Circuit and Programming

A simplified PAL structure is shown where the AND array has been programmed to generate three product terms which are added together by the OR array.

PALs have many inputs and multiple outputs connected through a large number of AND gates and OR gates. Drawing the circuit diagram of a PAL having multiple gates each having multiple inputs becomes difficult. PALs have Buffers at the inputs which produce the actual variable and its complement. The multiple input lines to an AND gate array are represented by a single line with a slash indicating the number of inputs. The cross indicates the fuses that are intact showing a connection between the vertical line and horizontal line of the AND array.

PAL Outputs

PALs typically have 8 or more inputs to the AND array and 8 or less outputs from the fixed OR array. Some PALs have combined inputs and outputs that can be programmed as either inputs or outputs. PAL output logic can be configured according to the application of the PAL. The modified block diagram representing a PAL showing the output of the OR Array connected to output logic which allows the outputs to be configured is shown in figure 19.11.

The three types of outputs are

- Combinational Output used for an SOP function and is available as an active-high or active-low output. Figure 19.12a
- Combinational Input/Output is used when the output is connected back to the input of the PAL or if the output pin is used as an input only. Figure 19.12b
- Programmable polarity output is used to either select the output function or its complement by programming an XOR gate at the output.

PAL Identification

PALs come in different configurations they are identified by unique number. The numbers begin with the prefix PAL followed by two digits that indicate the number of inputs followed by a letter L active-low, H active-high or P programmable polarity followed by a single or two digits that indicate the number of outputs. In addition to the standard number there may be suffixes which specify the speed, package type and temperature range.

Lecture No 20

Implementing Odd-Prime Number Function

The Odd-Prime Number generator can be implemented by programming the 4 x 3 PLA. Due to the limitations of the PLA which only has six product term (six AND gates), only the first six Odd-Prime numbers 1, 3, 5, 7, 11 and 13 can be detected. Additional two outputs are programmed to detect Odd-Prime multiples of 15 and 39 respectively. The six product terms represented by P1, P2, P3, P4, P5 and P6 are minterms 1, 3, 5, 7, 11 and 13. The first OR gate sums the six minterms (product terms) to give an output of 1 when any one of the first six
Odd-Prime numbers is applied at the inputs I1, I2, I3 and I4 of the PLA respectively. The second OR gate sums the minterms 1, 3 and 5. Thus the output of the second OR gate is a 1 when any of the three minterms is applied at the PLA inputs. Similarly, the third OR gate sums the minterms 1, 3 and 13 and the output is set to logic 1 when any one of the three inputs are detected at the input of the PLA.

GAL Operation: The GAL has a reprogrammable AND gate array and a fixed OR array. GAL can be reprogrammed as instead of fuses E^2CMOS logic is used which can be programmed to connect a column with a row. The E^2CMOS logic at each column–row intersection is known as a cell. The E^2CMOS cell in the 'on' state connects the column with the row and a cell in the 'off' state disconnects the column and row. Appropriate cells are programmed to the 'on' state to allow appropriate literals to be connected to the AND gates which generate product terms. The simplified GAL structure shows the implementation of an SOP function.

Programming of PLDs: PLDs are programmed with the help of computer which runs the programming software. The computer is connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board. The programming of a PLD device involves entering the logic function in the form of a Boolean equation, truth table or a state diagram. Any errors during the entry process are corrected. The software compiler processes the information in the input file and translates it into a suitable format. The complier also minimizes the logic. The minimized logic is then tested by using a set of hypothetical inputs known as test vectors. The testing verifies the design of the logic circuit before committing it to the PLD. If any flaws are detected during the testing process the design must be debugged and submitted for recompilation. Once the design has been finalized a documentation file is produced along with a fuse map file which is downloaded to the programmer which programs the PLD device inserted in the programmer socket.

PLDs have In-System Programming (ISP) capability that allows the PLDs to be programmed after they have been installed on a circuit board. A standard 4-wire interface is used for programming the In-System PLD. ISP capability allows systems to be upgraded by reprogramming the PLD.

The GAL22V10

The GAL22V10 is a popular GAL device having twelve inputs and ten inputs/outputs. The device is available as low-voltage 3.3v version. It is also available as an ISP version. The device has ten OLMCs that can be programmed to different output modes. The ten OLMCs receive different number of inputs from the programmable AND gate array.
The four OLMC configurations are

- Combination Mode with active-low output
- Combinational Mode with active-high output
- Registered Mode with active-low output
- Registered Mode with active-high output

OLMC Combinational Mode

When the select inputs S_0 and S_1 are set to 0 and 1 respectively, the 4-to-1 MUX selects the OR gate output and the output is active-low because of the inversion by the tristate buffer. When the select inputs are set to 1 and 1 respectively, the MUX selects the complement of the OR gate output. The output of the OLMC is active-high due to double inversion.

Tri-State Buffers

Tri-State Buffer is a NOT gate with a control line that disconnects the output from the input. When the control line is high the buffer operates like a NOT gate and when the control line is low the output is disconnected from the output and high impedance is seen at the output. Tri-state buffers are used to disconnect the outputs of devices which are connected or share a common output line.

Introduction to ABEL:

ABEL which is an acronym for advanced Boolean expression language is a hardware description language used for implementing logic designs using PLDs. ABEL is a device-independent language and can be used to program any type of PLD.
ABEL is run on a computer connected to a PLD programmer which programs the PLD.
ABEL provides three different text-based methods for describing and entering a logic design.
The three methods are

- Boolean equations
- Truth tables
- State diagrams

The Boolean equations and the truth table method are used for combinational logic circuits. The state diagram is used specifically for sequential logic circuits. The Boolean equations and the truth table method can also be used for describing and entering sequential logic circuits.

Lecture No 21

THE GAL16V8

This device has eight inputs, two special function input pins and eight pins that can be used as inputs or output. The architecture of the GAL16V8 is similar to that of a PAL and it is designed to be programmed in one of the three available modes to emulate most of the existing PALs, thus replacing the PAL. The three modes in which PALs are programmed are

- Simple
- Complex
- Registered

The simple and complex modes are associated with the Combinational Logic whereas the Registered mode is associated with Sequential Logic.

OLMC for GAL16V8

The OLMC of the GAL16V8 is similar to the OLMC of the GAL22V10 with some enhancements. The main aspects of the GAL16V8 OLMC are

Tri-state Buffer and OLMC output pin

The tri-state buffer connecting the output of the OLMC circuit to the output pin is controlled through four different sources. The tri-state buffer control input can be connected in four different ways.

1. Connected to V_{cc}. The output is always enabled.
2. Connected to GND. The output is disabled and the output pin is configured as an input pin.
3. Connected to the external pin (11) which can be connected to V_{cc} or GND. The tri-state buffer is therefore controlled externally by applying an appropriate signal at the pin.
4. Connected to the output of one of the eight AND gates connected to the OLMC. Thus the tri-state buffer is controlled by a logical expression.

The output of the Sum of Product term

The OR gate used to implement the Sum-of-Product term has its output connected to the output pin thorough the tri-state buffer. The tri-state buffer is also connected to the output from the flip-flop. Thus either of the two inputs to the tri-state buffer can be selected. The output of the OR gate can also be programmed for output polarity by configuring the XOR gate connected at the output of the OR gate.

Simple Mode

In the Simple Mode the OLMC is configured as dedicated active combinational output or as dedicated input (limited to six). Three possible combinations of the Simple Mode are

- Combinational Output.
- Combinational Output with feedback to AND Array.
- Dedicated input.

Complex Mode

In this mode the OLMCs can be configured in two ways. In the complex Mode the tristate control is formed by a logical expression, this leaves seven product terms that can be used to form a sum-of product expression. Two possible combinations of the Complex Mode are

- Combinational Output.
- Combinational Input/Output.

Introduction to ABEL

ABEL which is an acronym for Advanced Boolean Expression Language is a hardware description language used for implementing logic designs using PLDs. ABEL is a deviceindependent language and can be used to program any type of PLD. ABEL is run on a computer connected to a PLD programmer which programs the PLD. ABEL provides three different text-based methods for describing and entering a logic design. The three methods are

- Boolean Equations
- Truth Tables
- State Diagrams

The Boolean Equations and the Truth Table method are used for Combinational Logic Circuits. The State Diagram is used specifically for Sequential Logic circuits. The Boolean Equations and the Truth Table method can also be used for describing and entering Sequential Logic Circuits.

Boolean Operations and Boolean Notations

The NOT, AND, OR and XOR operations have special symbols in ABEL as shown in

Logic Operation	ABEL Symbol
NOT	!
AND	&
OR	#
XOR	

The standard Boolean notations in terms of ABEL notations are defined in table 20.2. The operators !, &, # and $ have precedence in the order given in table.

Boolean Notation	ABEL Symbol
$\bar{A}$	!A
A.B	A&B
A +B	A#B
A ⊕B	A$B

Boolean Equations

One of the ABEL entry methods uses logic equations. In ABEL any letter or combination of letters and numbers can be used to identify variables. ABEL however is casesensitive, thus variable 'A' is treated separately from variable 'a'. All ABEL equations must end
with ';'.

Boolean expression F = A$\bar{B}$ + AC +$\overline{BD}$ ABEL expression F = A & !B # A & C # !B & !D;

Multiple Inputs and Outputs

In some cases, multiple input and output variables can be grouped as a set to simplify an equation. Fig 21.7. Thus D_0, D_1 and D_2 input or output variables can be defined by a single variable D using the ABEL notation D = [D0, D1, D2];

The four ABEL notations can be represented by a single notation if variables A3, A2, A1 and A0 are defined as a set A. Similarly, sets B, C and D can be defined.

Truth Table

ABEL accepts a logical design described in the form of a Truth Table. Truth Tables are sometimes more convenient in describing certain logic circuits. The ABEL Truth Table format includes a header and the truth table entries.
TRUTH_TABLE ([A, B, C, D] → [X1, X2]) A, B, C and D are the inputs and XI and X2 are the outputs.
The truth table of an XOR gate is represented by the ABEL Truth Table notation.

Test Vectors

Once the Logic circuit design has been entered its operation is verified by using 'test vectors'. A 'test vector' specifies the inputs and the corresponding outputs. The software simulates the operation of the logic circuit by applying the test vector and checking the outputs. Test vectors are essentially the same as Truth Tables.

The ABEL Input File

When an Input (source) file is created in ABEL a module is created which has three sections. The three sections are

Declarations

The declaration section generally includes the device declaration, pin declarations and set declarations. Device declaration is used to specify the PLD device that is to be programmed. The device is referred to as the target device. Decoder device 'P22V10'; A0, A1, A2, A3, PIN 1, 2, 3, 4; INPUT = [A1, A0, B1, B0];

Logic Descriptions

Logic descriptions include the three methods of describing a logic circuit. Two methods

Test Vectors

The Test Vector format has been described. The Test vector description is used to simulate the logic circuit and verify its operation. the Boolean equation and the Truth Table method already have been discussed.

The Documentation file

After an input file is processed by ABEL a documentation file is generated which provides a hardcopy of the final reduced equations, a JEDEC file and a device pin diagram.

The JEDEC file

The JEDEC file is downloaded to the PLD programmer to program the appropriate PLD device.

Lecture No 22

A Quad 1-of-4 MUX has four Multiplexers, each Multiplexer has four inputs and a single output. Each multiplexer has two select inputs to select one of the four inputs. The two select inputs are common to all the four multiplexers. The function table of the Quad 1-of-4 MUX is shown in table 22.1.

Select Inputs		Outputs			
S_1	S_0	D_{out}	C_{out}	B_{out}	A_{out}

0	0	D_0	C_0	B_0	A_0
0	1	D_1	C_1	B_1	A_1
1	0	D_2	C_2	B_2	A_2
1	1	D_3	C_3	B_3	A_3

Table 22.1 Truth table of a Quad 1-of-4 Multiplexer

```
Module quad_1of4_mux
Title          'Quad 1 of 4 multiplexer in a GAL20V8'
       mux    device          'P20V8';
       A0, A1, A2, A3          pin 1, 2, 3, 4;
       B0, B1, B2, B3          pin 5, 6, 7, 8;
       C0, C1, C2, C3          pin 9, 10, 11, 13;
       D0, D1, D2, D3          pin 14, 15, 16, 17;
       Aout, Bout, Cout, Dout  pin 21, 20, 19, 18;
S0, S1                         pin 22, 23;
Equations
       Aout = !S1 & !S0 & A0 # !S1 & S0 & A1 # S1& !S0 & A2 # S1 & S0 & A3;
       Bout = !S1 & !S0 & B0 # !S1 & S0 & B1 # S1& !S0 & B2 # S1 & S0 & B3;
       Cout = !S1 & !S0 & C0 # !S1 & S0 & C1 # S1& !S0 & C2 # S1 & S0 & C3;
       Dout = !S1 & !S0 & D0 # !S1 & S0 & D1 # S1& !S0 & D2 # S1 & S0 & D3;
Test_vectors
([S1, S0, A0, A1, A2, A3, B0, B1, B2, B3, C0, C1, C2, C3, D0, D1, D2, D3] →
[Aout, Bout, Cout, Dout])
"S  S  A  A  A  A  B  B  B  B  C  C  C  C  D  D  D  D  outputs
"0  1  0  1  2  3  0  1  2  3  0  1  2  3  0  1  2  3        A  B  C  D
[0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1] →  [1, 0, 0, 0];
[0, 1, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1] →  [0, 1, 0, 0];
[1, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1] →  [0, 0, 1, 0];
[1, 1, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 0, 0, 1] →  [0, 0, 0, 1];
[0, 0, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 1] →  [1, 1, 1, 0];
[0, 1, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 1] →  [1, 1, 0, 1];
[1, 0, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 1] →  [1, 0, 1, 1];
[1, 1, 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 1] →  [0, 1, 1, 1];
```

Implementation of Quad MUX: The Quad Multiplexer has 16 inputs, 4 inputs for each Multiplexer. Each multiplexer has a single output, therefore a total of 4 outputs are required. To select an appropriate multiplexer input there are two select input lines connected to all the four multiplexers. The Quad Multiplexer has a total of 22 pins through which the device is operated. The GAL16V8 device can not be used as it does not enough pins to implement the quad multiplexer. The GAL20V8 PLD is used for the implementation of the Quad 1-of-4 Multiplexer. The device has 12 inputs, 2 special function inputs and 8 input/output pins. Four input/output pins of the GAL device are configured as inputs to support the fourth multiplexer inputs D1, D2 and D3 and the select input S0.

Sequential Circuits: The combinational digital circuits have no storage element; therefore combinational circuits handle only instantaneous inputs. The outputs of the combinational circuits also can not be stored. The absence of a memory element restricts the use of digital combinational circuits to certain application areas. The use of a memory element which is capable of storing digital inputs and outputs is an important part of all practical digital circuits.

Consider an ALU which performs Arithmetic and Logical operations. An ALU can not perform its operations unless it is connected to memory elements that store the inputs applied at the inputs of the ALU and outputs from the ALU. Consider an ALU that performs addition operation on a set of numbers, 2, 3, 4 and 5. The ALU can add two numbers at a time; therefore the ALU has to add the four numbers two at a time. The four numbers have to be stored temporarily, the partial results after adding two numbers also need to be stored. To add the four numbers, the first two numbers 2 and 3 stored in two separate memory elements are added together, the result (5) has to be added to the next number 4. The result (5) is temporarily stored in one of the two memory elements used to store the numbers 2 and 3. The result (5) is added to the third number 4 to provide another partial sum result 9 which has to be stored and then added with the fourth number 5.

In a parallel-to-serial conversion of byte data using a multiplexer and the conversion from serial-to-parallel using a demultiplexer, memory elements are required that store the byte data at the input of the multiplexer for conversion into serial information and another memory element at the output of the demultiplexer for conversion back to parallel.

The counter circuit used in digital circuits count to the next value because of the memory element which stores and remembers the previous count value. A counter can not operate without a memory element.

Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.

Latches and Flip-Flops: A latch is a temporary storage device that has two stable states. A latch output can change from one state to the other by applying appropriate inputs. A latch normally has two inputs, the binary inputcombinations at the latch input allows the latch to change its state. A latch has two outputs Q and its complement $\overline{Q}$. The latch is said to be in logic high state when Q=1 and $\overline{Q}$=0 and it is in the logic low state when Q=0 and $\overline{Q}$=1. When the latch is set to a certain state it retains its state unless the inputs are changed to set the latch to a new state. Thus a latch is a memory element which is able to retain the information stored in it.

The NAND gate based S-R (Set-Reset) Latch: An S-R Latch is implemented by connecting two NAND gates together. The output of each NAND gate is connected to the input of the other NAND gate. The unconnected inputs of the two NAND gates are the Set S and Reset R inputs. The outputs of the two NAND gates are the Q and its complement $\overline{Q}$.

The S-R latch has two inputs, therefore four different combinations of inputs can be applied to control the operation of the S-R latch. The four possible input combinations are

1. Inputs S=0 & R=0

a. Assume that the outputs Q and $\overline{Q}$ are set at logic 1 and logic 0 respectively. Since both the inputs S and R are logic low, therefore both the Q and $\overline{Q}$ outputs are set to 1. The inputs S = 0 and R = 0 are never applied as these inputs result in invalid output states as Q and $\overline{Q}$ should be complements of each other.

b. Assume that the outputs Q and $\overline{Q}$ are set at logic 0 and logic 1 respectively. Since both the inputs S and R are logic low, therefore both the Q and $\overline{Q}$ outputs are set to 1. The inputs S = 0 and R = 0 are never applied as these inputs result in invalid output states as Q and $\overline{Q}$ should be complements of each other.

The input combination S=0 and R=0 is considered to be invalid as it results in an invalid output of Q=1 and $\overline{Q}$=1.

2. Inputs S=0 & R=1

a. Consider that the outputs Q and $\overline{Q}$ have 1 and 0 logic states. The Set input S = 0 sets the output Q to 1. The Q input and the R inputs to gate 2 are both at logic 1, therefore the output $\overline{Q}$ is set to 0.

b. Consider that initially the Q and $\overline{Q}$ outputs are at logic state 0 and 1 respectively. The Set input S = 0 sets the output Q to 1. The Q input and the R inputs to gate 2 are both at logic 1, therefore the output $\overline{Q}$ is set to 0.

Thus what ever the initial outputs, setting S to 0 and R to 1 sets the Q and $\overline{Q}$ outputs to 1 and 0 respectively.

3. Inputs S=1 & R=0

a. Initially, the Q and $\overline{Q}$ outputs are at 1 and 0 respectively. The Reset input R=0 sets the output $\overline{Q}$ to 1. The inputs of gate 1, $\overline{Q}$ and S are both at logic 1, therefore the output Q is set to 0.

b. Initially, if the Q and $\overline{Q}$ outputs are at logic 0 and 1 respectively, setting R to 0 sets $\overline{Q}$ to 1. The inputs of gate 1, $\overline{Q}$ and S are both at logic 1, therefore the output Q is set to 0.

Thus, what ever the outputs, setting S to 1 and R to 0 sets the Q and $\overline{Q}$ outputs to 0 and 1 respectively.

4. Inputs S=1 & R=1

a. Initially, the Q and $\overline{Q}$ outputs are at 1 and 0 respectively. The inputs of gate 2 , Q and R are both at logic 1, therefore the output $\overline{Q}$ is set to 0. The inputs of gate 1, $\overline{Q}$ and S are 0 and 1 respectively, therefore the output is set to 1.

b. Initially, the Q and $\overline{Q}$ outputs are at 0 and 1 respectively. The inputs of gate 2 , Q and R are at logic 0 and 1 respectively, therefore the output $\overline{Q}$ is set to 1. The inputs of gate 1, $\overline{Q}$ and S are both at logic 1 respectively, therefore the output is set to 0.

Thus, with S and R inputs both set to logic 1, the previous output state is maintained. If initially, the Q and $\overline{Q}$ are at logic 1 and 0 respectively, setting S=1 and R=1 maintains the same outputs. Similarly, if initially Q and $\overline{Q}$ are at logic 0 and 1 respectively, setting S=1 and R=1 maintains the same outputs.

The NOR gate based S-R (Set-Reset) Latch: A NOR based S-R latch is implemented using NOR gates instead of NAND gates. Connections are identical to that of the NAND based latch. The S and R inputs have been switched.

The S-R NOR based latch has two inputs, therefore four different combinations of inputs can be applied to control the operation of the S-R latch. The four possible input combinations are

1. Inputs S=0 & R=0

a. Assume that the outputs Q and $\overline{Q}$ are set at logic 1 and logic 0 respectively. The R and $\overline{Q}$ inputs at gate 1 are both at logic 0, therefore the Q output is set to logic 1. The S and Q inputs at gate 2 are at logic 0 and 1 respectively, therefore the output $\overline{Q}$ is set to logic 0.

b. Assume that the outputs Q and $\overline{Q}$ are set at logic 0 and logic 1 respectively. The S and Q inputs at gate 2 are both at logic 0, therefore the $\overline{Q}$ output is set to logic 1. The R and $\overline{Q}$ inputs at gate 1 are at logic 0 and 1 respectively, therefore the output Q is set to logic 0.

Thus, with S and R inputs both set to logic 0, the previous output state is maintained. If initially, the Q and $\overline{Q}$ are at logic 1 and 0 respectively, setting S=0 and R=0 maintains the same outputs. Similarly, if initially Q and $\overline{Q}$ are at logic 0 and 1 respectively, setting S=0 and R=0 maintains the same outputs.

2. Inputs S=0 & R=1

a. Consider that the outputs Q and $\overline{Q}$ have 1 and 0 logic states. The Reset input R = 1 sets the output Q to 0. The Q input and the S inputs to gate 2 are both at logic 0, therefore the output $\overline{Q}$ is set to 1.

b. Consider that initially the Q and $\overline{Q}$ outputs are at logic state 0 and 1 respectively. The Reset input R = 1 sets the output Q to 0. The Q input and the S inputs to gate 2 are both at logic 0, therefore the output $\overline{Q}$ is set to 1.

Thus what ever the initial outputs, setting S to 0 and R to 1 sets the Q and $\overline{Q}$ outputs to 0 and 1 respectively.

3. Inputs S=1 & R=0

a. Initially, the Q and $\overline{Q}$ outputs are at 1 and 0 respectively. The Set input S=1 sets the output $\overline{Q}$ to 0. The inputs of gate 1, $\overline{Q}$ and R are both at logic 0, therefore the output Q is set to 1.

b. Initially, if the Q and $\overline{Q}$ outputs are at logic 0 and 1 respectively, setting S to 1 sets $\overline{Q}$ to 0. The inputs of gate 1, $\overline{Q}$ and R are both at logic 0, therefore the output Q is set to 1.

Thus, what ever the outputs, setting S to 1 and R to 0 sets the Q and $\overline{Q}$ outputs to 1 and 0 respectively.

4. Inputs S=1 & R=1

a. Initially, the Q and $\overline{Q}$ outputs are at 1 and 0 respectively. Since both the inputs S and R are logic 1, therefore both the Q and $\overline{Q}$ outputs are set to 0. The inputs S = 1 and R = 1 are never applied as these inputs result in invalid output states as Q and $\overline{Q}$ should be complements of each other.

b. Initially, the Q and $\overline{Q}$ outputs are at 0 and 1 respectively. Since both the inputs S and R are logic 1, therefore both the Q and $\overline{Q}$ outputs are set to 0. The inputs S = 1 and R = 1 are never applied as these inputs result in invalid output states as Q and $\overline{Q}$ should be complements of each other.

The input combination S=1 and R=1 is considered to be invalid as it results in an invalid output of Q=0 and $\overline{Q}$=0.

S-R Latch Timing Diagrams: The operation of the active-high and active-low input latches can be understood with the help of timing diagrams. Figure 22.6 shows the timing diagrams of the active high and active-low input latches respectively. In the timing diagram of the NAND based S-R flip-flop, the inputs S=0 and R=0 are not applied as it results in an invalid output state. Similarly, in the timing diagram of the NOR based S-R flip-flop, the inputs S=1 and R=1 are not applied as it results in an invalid output state.

CS302 Quiz 1 Solution by MCS of Virtuallians

MCS of Virtuallians Group Team

1. The terminal count of a 4-bit binary counter in the UP mode is _____.
    a. 1100
    b. 0011
    c. 1111
    d. 0000
2. For a down counter that counts from (111 to 000). If current state is "101" the next state will be _____.
    a. 111
    b. 110
    c. 010
    d. None of given options
3. The n flip-flops store _____ states.
    a. 1
    b. 2^n
    c. 0
    d. 2^(n+1)
4. An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting _____.
    a. Q output of all flip-flops to clock input of next flip-flops
    b. Q' output of all flip-flops to clock input of next flip-flops
    c. Q output of all flip-flops to J input of next flip-flops
    d. Q' output of all flip-flops to K input of next flip-flops
5. In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together.
    a. True
    b. False
6. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.
    a. True
    b. False
7. The 74HC163 is a 4-bit Synchronous Counter, it has _____ data output pins.
    a. 2
    b. 4
    c. 6
    d. 8
8. _____ Counters as the name indicates are not triggered simultaneously
    a. Asynchronous
    b. Synchronous
    c. Positive-Edge triggered
    d. Negative-Edge triggered
9. Divide-by-32 counter can be achieved by using

a. Flip-Flop and DIV 10
b. Flip-Flop and DIV 16
c. Flip-Flop and DIV 32
d. DIV 16 and DIV 32

10. The _____ input overrides the _____ input
a. Asynchronous, synchronous
b. Synchronous, asynchronous
c. Preset input (PRE), Clear input (CLR)
d. Clear input (CLR), Preset input (PRE)

11. The synchronous counters are also known as Ripple Counters:
a. True
b. False

12. Each stage of Master-slave flip-flop works at _____ of the clock signal
a. Each stage works on complete clock signal
b. One fourth
c. One third
d. One half

13. With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in
a. 80 micro seconds
b. 8 micro seconds
c. 80 mili seconds
d. 10 micro seconds

14. Number of states in an 8-bit Johnson counter sequence are:
a. 8
b. 12
c. 14
d. 16

15. A synchronous decade counter will have _____ flip-flops
a. 3
b. 4
c. 7
d. 10

16. _____ is one of the examples of synchronous inputs.
a. J-K input
b. EN input
c. Preset input (PRE)
d. Clear input (CLR)

17. A decade counter is _____
a. Mod-3 counter
b. Mod-5 counter
c. Mod-8 counter
d. Mod-10 counter

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18. _____ is said to occur when multiple internal variables change due to change in one input variable
    a. Hold and Wait
    b. Clock Skew
    c. Race condition
    d. Hold delay
19. In moore machine the output depends on
    a. The current state and the output of previous flip flop
    b. Only inputs
    c. The current state
    d. The current state and inputs
20. Asynchronous mean that _____
    a. Each flip-flop after the first one is enabled by the output of the preceding flip-flop
    b. Each flip-flop is enabled by the output of the preceding flip-flop
    c. Each flip-flop except the last one is enabled by the output of the preceding flip-flop
    d. Each alternative flip-flop after the first one is enabled by the output of the preceding flip-flop
21. Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
    a. Ten
    b. Eight
    c. Three
    d. Two
22. A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
    a. 3
    b. 7
    c. 8
    d. 15
23. According to moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.
    a. Previous state
    b. Present state
    c. Next state
    d. External inputs
24. In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?
    a. Qt
    b. 0
    c. 1
    d. Invalid
25. A Divide-by-20 counter can be achieved by using
    a. Flip-Flop and DIV 10
    b. Flip-Flop and DIV 16

c. Flip-Flop and DIV 32
d. DIV 10 and DIV 16

26. We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using _____.
    a. Using S-R Flop-Flop
    b. D-flipflop
    c. J-K flip-flop
    d. T-Flip-Flop
27. A one-shot mono-stable device contains _____
    a. AND gate, Resistor, Capacitor and NOT Gate
    b. NAND gate, Resistor, Capacitor and NOT Gate
    c. NOR gate, Resistor, Capacitor and NOT Gate
    d. XNOR gate, Resistor, Capacitor and NOT Gate
28. The _____ inputs can be directly mapped to karnaugh maps.
    a. S-R
    b. J-K
    c. Flip-Flop
    d. External
29. A mono-stable device only has a single stable state
    a. True
    b. False
30. The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____
    a. Set-up time
    b. Hold time
    c. Pulse interval time
    d. Pulse stability time (PST)
31. The low to high or high to low transition of the clock is considered to be a(n) _____
    a. State
    b. Edge
    c. Trigger
    d. One-shot
32. A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state, on the next clock pulse, to what state does the counter go?
    a. 1001
    b. 1011
    c. 0011
    d. 1100
33. When the _____ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of _____ seconds.
    a. 1, 2

b. 0, 2
c. 2, 5
d. 1, 1

34. Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.
a. Set
b. Toggle
c. Latch
d. Reset

35. A stage in the shift register consists of
a. A latch
b. A flip flop
c. A byte of storage
d. Four bits of storage

36. When the both inputs of edge-triggered J-K flop-flop are set to logic zero _____
a. The flop-flop is triggered
b. Q=0 and Q'=1
c. Q=1 and Q'=0
d. The output of flip-flop remains unchanged

37. A positive edge-triggered flip-flop changes its state when _____
a. Enable input (EN) is set
b. Preset input (PRE) is set
c. Low-to-high transition of clock
d. High-to-low transition of clock

38. If a circuit suffers "Clock Skew" problem, the output of circuit can't be guarantied.
a. True
b. False

39. The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
a. Set-up time
b. Hold time
c. Pulse interval time
d. Pulse stability time (PST)

40. A modulus-14 counter has fourteen states requiring _____
a. 14 flip flops
b. 14 registers
c. 4 flip flops
d. 4 registers

41. In Master-Slave flip-flop the clock signal is connected to slave flip-flop using _____ gate.
a. AND
b. OR
c. NOT
d. NAND

42. _____ flip-flops are obsolete now.
    a. Edge-triggered
    b. Master-Slave
    c. T-flipflop
    d. D-flipflop
43. The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip flop _____
    a. Doesn't have an invalid state
    b. Sets to clear when both J=0 and K=0
    c. It does not show transition on change in pulse
    d. It does not accept asynchronous inputs
44. The glitches due to "Race Condition" can be avoided by using a _____.
    a. Gated flip-flops
    b. Pulse triggered flip-flops
    c. Positive-Edge triggered flip-flops
    d. Negative-Edge triggered flip-flops
45. For a gated D-Latch if EN=1 and D=1 then Q(t+1)=_____
    a. 0
    b. 1
    c. Q(t)
    d. Invalid
46. _____ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
    a. Race condition
    b. Clock skew
    c. Ripple effect
    d. None of given options
47. In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is _____
    a. 0000
    b. 1111
    c. 0001
    d. 10000
48. A 4-bit binary UP/DOWN counter is in the binary state zero, the next state in the DOWN mode is _____
    a. 0001
    b. 1111
    c. 1000
    d. 1110
49. An Astable multivibrator is known as a(n) _____.
    a. Oscillator
    b. Booster
    c. One-shot

d. Dual-shot

50. _____ is one of the examples of asynchronous inputs.
a. J-K input
b. S-R input
c. D input
d. Clear input (CLR)

51. In Master-Slave flip-flop setup, the master flip-flop operators at _____
a. Positive half cycle of pulse
b. Negative half cycle of pulse
c. Both Master-Slave operator simultaneously
d. Master-Slave flip-flop does not operate on pulses rather it is edge triggered

52. The power consumed by a flip-flop is defined by _____
a. P = Icc x Rcc
b. P = Vcc x Rcc
c. P = Vcc x Icc
d. P = Mcc x Vcc

53. In designing any counter the transition from a current state to the next state is determined by
a. Current state and inputs
b. Only inputs
c. Only current state
d. Current state and outputs

54. The 74HC163 is a 4-bit Synchronous Counter, it has _____ parallel data inputs pins
a. 2
b. 4
c. 6
d. 8

55. The 3-bit up counter can be implemented using _____ flip-flop(s).
a. S-R flip-flops only
b. S-R flip-flops and D-flip-flops
c. S-R flip-flops or D-flip-flops
d. D-flip-flop only

56. The terminal count of a modulus-13 binary counter is
a. 0000
b. 1111
c. 1101
d. 1100

57. The terminal count of a 4-bit binary counter in the DOWN mode is _____
a. 0000
b. 0011
c. 1100
d. 1111

58. In gated SR latch, what is the value of the output if EN=1, S=1 and R=0?
a. Qt

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b. 0
c. 1
d. Invalid

59. In gated SR latch, what is the value of the output if EN=1, S=0 and R=0?
a. Qt
b. 0
c. 1
d. Invalid

60. Which mechanism allocate the binary values to the states in order to reduce the cost of the combinational circuits?
a. State reduction
b. State minimization
c. State assignment
d. State evaluation

61. State of flip-flop can be switched by changing its _____
a. Input signal
b. Output signal
c. Momentary signal
d. Contemporary signal

62. Once the state diagram is drawn for any sequential circuit the next step is to draw
a. Transiation table
b. Karnaugh map
c. Next-state table
d. Logic expression

63. Design of state diagram is one of many steps used to design
a. A clock
b. A truncated counter
c. An UP/DOWN counter
d. Any counter

64. Flip flops are also called _____
a. Bi-stable multivibrators
b. Bi-stable singlevibrators
c. Bi-stable dualvibrators
d. Bi-stable transformer

65. Three cascaded modulus-10 counters have an overall modulus of
a. 30
b. 100
c. 1000
d. 10000

66. In mealy machine the output depends on
a. The inputs
b. The current state
c. Current state and the inputs

d. None of the above

67. If S=1 and R=0, then for positive edge triggered flip-flop Q(t+1) = _____
    a. 0
    b. 1
    c. Invalid
    d. Input is invalid

68. The term hold always means _____.
    a. Q=0, Q'=1
    b. Q=1, Q'=0
    c. Q=0, Q'=0
    d. No change

69. A transparent mode means _____
    a. The changes in the data at the inputs of the latch are seen at the output
    b. The changes in the data at the inputs of the latch are not seen at the output
    c. Propagation delay is zero (output is immediately changed when clock signal is applied)
    d. Input hold time is zero (no need to maintain input after clock ttransition)

70. A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?
    a. J=1, K=0
    b. J=1, K=X(Don't care)
    c. J=X(Don't care), K=0
    d. J=0, K=X(Don't care)

71. To parallel load a byte of data into a shift register, there must be
    a. One clock pulse
    b. One clock pulse for each 1 in the data
    c. Eight clock pulse
    d. One clock pulse for each 0 in the data

72.

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CS302- Digital Logic Design

Question No: 1 (Marks: 1) - Please choose one

The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

- 8-bit
- 16-bit
- **32-bit (Page 25)**
- 64-bit

Question No: 2 (Marks: 1) - Please choose one

The decimal "17" in BCD will be represented as _____

- 11101
- 11011
- **10111**
- 11110

Question No: 3 (Marks: 1) - Please choose one

The basic building block for a logical circuit is _____

- A Flip-Flop
- **A Logical Gate (Page 7)**
- An Adder
- None of given options

Question No: 4 (Marks: 1) - Please choose one

The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

- Undefined
- One
- **Zero (According to rule)**
- No Output as input is invalid.

Question No: 5 (Marks: 1) - Please choose one

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

- 2
- 8
- **12 (According to rule "2^n")**
- 16

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Question No: 6 (Marks: 1) - Please choose one

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

- **AND (Page 182)**
- OR
- NOT
- XOR

Question No: 7 (Marks: 1) - Please choose one

_____ is one of the examples of synchronous inputs.

- **J-K input (Page 235)**
- EN input
- Preset input (PRE)
- Clear Input (CLR)

Question No: 8 (Marks: 1) - Please choose one

_____ is one of the examples of asynchronous inputs.

- J-K input
- S-R input
- D input
- **Clear Input (CLR) (Page 235)**

Question No: 9 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

- **Asynchronous, synchronous (Page 369)**
- Synchronous, asynchronous
- Preset input (PRE), Clear input (CLR)
- Clear input (CLR), Preset input (PRE)

Question No: 10 (Marks: 1) - Please choose one

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- Race condition
- **Clock Skew (Page 226)**
- Ripple Effect
- None of given options

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Question No: 11 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

- 0000
- **1101**
- 1011
- 1111

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

- **Current state and the inputs (Page 232)**
- Current state and outputs
- Previous state and inputs
- Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

- **State assignment (Page 341)**
- State reduction
- Next state table
- State diagram

Question No: 14 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- State diagram
- Next state table
- State reduction
- **State assignment (Page 335)**

Question No: 15 (Marks: 1) - Please choose one

The best state assignment tends to _____.

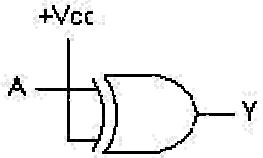
- **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
- Minimizes the number of state variables that don"t change in a group of related states
- Minimize the equivalent states
- None of given options

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Question No: 16 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- 1
- 0
- **A**
- $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- 1
- 2
- 4
- **8 (Page 356)**

Question No: 18 (Marks: 1) - Please choose one
5-bit Johnson counter sequences through ____ states

- 7
- **10 (Page 354)**
- 32
- 25

uestion No: 19 (Marks: 1) - Please choose one
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- 1100
- 0011
- **0000**
- 1111

Question No: 20 (Marks: 1) - Please choose one
The address from which the data is read, is provided by _____

- Depends on circuitry
- None of given options
- RAM
- **Microprocessor (Page 397)**

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Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- **First In, First Out (Page 424)**
- Fly in, Fly Out
- Fast in, Fast Out
- None of given options

Question No: 22 (Marks: 1) - Please choose one

LUT is acronym for _____

- **Look Up Table (Page 439)**
- Local User Terminal
- Least Upper Time Period
- None of given options

Question No: 23 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

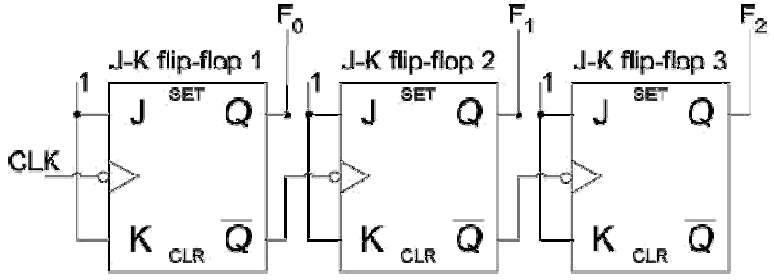
- **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
- $V_{out} / R_f = - V_{in} / R_i$
- $R_f / V_{in} = - R_i / V_{out}$
- $R_f / V_{in} = R_i / V_{out}$

Question No: 24 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

- Resolution
- **Accuracy (Page 460)**
- Quantization
- Missing Code

Question No: 25 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- **Asynchronous up-counter (Page 270)**
- Asynchronous down-counter
- Synchronous up-counter
- Synchronous down-counter

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Question No: 26 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354)**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

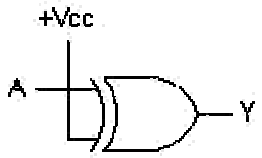
Question No: 27 (Marks: 1) - Please choose one

A synchronous decade counter will have _____ flip-flops

► 3
► **4 (Page 281)**
► 7
► 10

Question No: 28 (Marks: 1) - Please choose one

The output of this circuit is always _____.



► 1
► 0
► **A**
► $\overline{A}$

Question No: 24 (Marks: 1) - Please choose one

At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

► 2
► 4
► 6
► **8**

Question No: 25 (Marks: 1) - Please choose one

In _____ the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

► Moore machine
► Mealy machine
► **Johnson counter (Page 354)**
► Ring counter

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Question No: 26 (Marks: 1) - Please choose one

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

- Moore machine
- Meally machine
- Johnson counter
- **Ring counter (Page 355)**

Question No: 27 (Marks: 1) - Please choose one

Which is not characteristic of a shift register?

- **Serial in/parallel in (Page 346)**
- Serial in/parallel out
- Parallel in/serial out
- Parallel in/parallel out

Question No: 28 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- **1100**
- 0011
- **0000**
- 1111

Question No: 29 (Marks: 1) - Please choose one

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

- Write Time
- Recycle Time
- Refresh Time
- **Access Time (Page 417)**

Question No: 30 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- n+2 (n plus 2)
- **2n (n multiplied by 2) (Page 354)**
- 2^n (2 raise to power n)
- n^2 (n raise to power 2)

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Question No: 31 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
- FALSE
- **TRUE (Page 250)**

Question No: 32 (Marks: 1) - Please choose one
The output of an XNOR gate is 1 when _____
I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one
- I Only
- IV Only
- I and IV only
- **II and III only (Page 53)**

Question No: 33 (Marks: 1) - Please choose one
NAND gate is formed by connecting _____
- **AND Gate and then NOT Gate (Page 45)**
- NOT Gate and then AND Gate
- AND Gate and then OR Gate
- OR Gate and then AND Gate

Question No: 34 (Marks: 1) - Please choose one
Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____
- Zero
- **One (Page 46)**
- Undefined
- No output as input is invalid

Question No: 35 (Marks: 1) - Please choose one
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____
- Radiation-Erase programming method (REPM)
- **In-System Programming (ISP) (Page 194)**
- In-chip Programming (ICP)
- Electronically-Erase programming method(EEPM)

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Question No: 36 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is
- !
- &
- **# (Page 201)**
- $

Question No: 37 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
- 0
- 1
- **Invalid (Page 230)**
- Input is invalid

Question No: 38 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____
- **Doesn't have an invalid state (Page 232)**
- Sets to clear when both J = 0 and K = 0
- It does not show transition on change in pulse
- It does not accept asynchronous inputs

Question No: 39 (Marks: 1) - Please choose one
For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____
- 0
- **1 (Page 227)**
- Q(t)
- Invalid

Question No: 40 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock
- True
- **False (Page 245)**

Question No: 41 (Marks: 1)
In the statement "X PIN 22 ISTYPE 'reg.buffer"
What is the meaning of the keyword "reg.buffer"

Question No: 42 (Marks: 1)
What are the two basic operations which are performed on memory?

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Question No: 43 (Marks: 2)

Explain state assignment process.

Question No: 44 (Marks: 2)

What is RAM Stack, which register stores the address of the top of the stack?

Question No: 45 (Marks: 3)

How can we calculate the frequency of an unknown signal?

Question No: 46 (Marks: 3)

Explain dynamic RAM in your own words.

Question No: 47 (Marks: 3)

Suppose a 2 bit up-down counter having states "A, B, C, D". the counter counts upward when X=1 and downward when X=0. Write down IF-THEN-ELSE statements to show how present states change to next states and previous states.

Question No: 48 (Marks: 5)

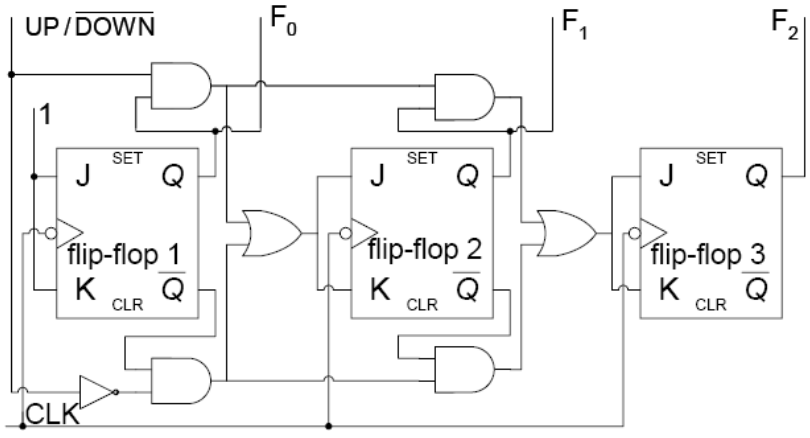
Explain memory read operation with the help of an example.

Question No: 49 (Marks: 5)

Draw the next-state table of any sequential counter with the help of J-K flip flop transition

Question No: 50 (Marks: 10)

You are given the diagram of up-down counter; explain how it works as an up and down counter.

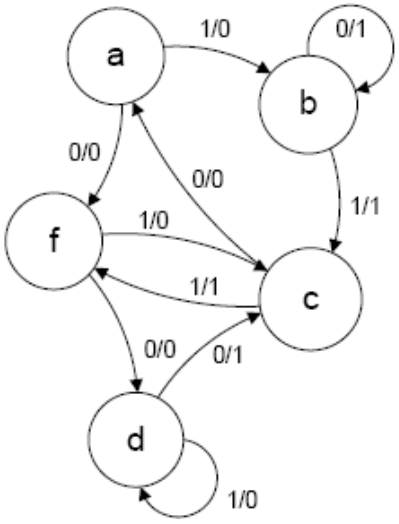


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Question No: 51 (Marks: 10)

Consider a state sequence a, b, c, f, d, d, c, f, d, c, a, f, d, c. Starting from initial state a, draw a table for the inputs and outputs for the state diagram given below (up to first ten transitions).



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Hearthacker124@gmail.com

Paper # 1

MIDTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design

Time: 60 min
Marks: 38

Question No: 1 (Marks: 1) - Please choose one

A SOP expression is equal to 1 _____

- All the variables in domain of expression are present
- At least one variable in domain of expression is present.

► When one or more product terms in the expression are equal to 0.

► When one or more product terms in the expression are equal to 1. Page86

Question No: 2 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10

Question No: 3 (Marks: 1) - Please choose one

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► True
► False

Question No: 4 (Marks: 1) - Please choose one

High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► 0.9 V
► 3.3 V

Question No: 5 (Marks: 1) - Please choose one

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582
► 2.4582
► 24582
► 0.24582

Question No: 6 (Marks: 1) - Please choose one

The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined
► One
► Zero
► 10 (binary)

Question No: 7 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET
► RESET
► Clear
► Invalid

Question No: 8 (Marks: 1) - Please choose one

3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► Fast switching speeds, very low power dissipation
page61
► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) - Please choose one

The binary value "1010110" is equivalent to decimal _____

► 86
► 87
► 88
► 89

Question No: 10 (Marks: 1) - Please choose one

The _____ Encoder is used as a keypad encoder.

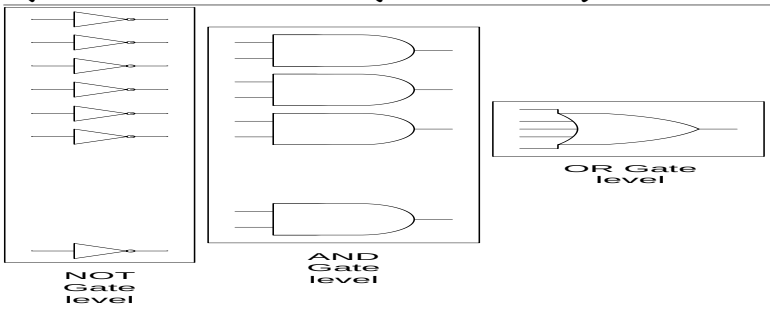
► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► Decimal-to-BCD Priority

Question No: 11 (Marks: 1) - Please choose one

How many data select lines are required for selecting eight inputs?

- ▶ 1
- ▶ 2
- ▶ 3
- ▶ 4

Question No: 12 (Marks: 1) - Please choose one



the diagram above shows the general implementation of _____ form

- ▶ Boolean
- ▶ Arbitrary
- ▶ POS page122
- ▶ SOP

Question No: 13 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

- ▶ 4
- ▶ 8
- ▶ 12
- ▶ 16

Question No: 14 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs.**
► Multiple inputs and single output.

Question No: 15 (Marks: 1) - Please choose one

The expression _____ is an example of Commutative Law for Multiplication.

► $AB+C = A+BC$
► $A(B+C) = B(A+C)$
► **$AB=BA$**
► $A+B=B+A$

Question No: 16 (Marks: 1) - Please choose one

"Sum-of-Weights" method is used _____

► **to convert from one number system to other**
► to encode data
► to decode data
► to convert from serial to parallel data

Question No: 17 (Marks: 2)

Why a 2-bit comparator is called parallel comparator?

Answer:

The 2-bit Comparator discussed earlier is considered to be a Parallel Comparator as all the bits are compared simultaneously. External Logic has to be used to Cascade together two such Comparators to form a 4-bit Comparator.

Question No: 18 (Marks: 2)

Explain at least two advantages of the circuit having low power consumption :

Answer:

Power Dissipation

Logic Gates and Logic circuits consume varying amount of power during their operation.

Ideally, logic gates and logic circuit should consume minimal power. Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries use Integrated circuits that have low power dissipation. Secondly, low power consumption means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices.

Microprocessors for example generate considerable heat which has to be dissipated by mounting small fans. Generally, the Power dissipation of TTL devices remains constant throughout their operation. CMOS device on the other hand dissipate varying amount power depending upon the frequency of operation.

Question No: 19 (Marks: 2)

Name the four OLMC configurations

Answer:

The four OLMC configurations are

- Combination Mode with active-low output
- Combinational Mode with active-high output
- Registered Mode with active-low output
- Registered Mode with active-high output

Question No: 20 (Marks: 3)

Explain "Test Vector" in context of ABEL

Answer:

The programming of a PLD device involves entering the logic function in the form of a Boolean equation, truth table or a state diagram. Any errors during the entry process are corrected. The software compiler processes the information in the input file and translates it into a suitable format. The complier also minimizes the logic. The minimized logic is then tested by using a set of hypothetical inputs known as test vectors. The testing verifies the design of the logic circuit before committing it to the PLD.

Question No: 22 (Marks: 5)

Explain Tri-State Buffers with the help of block diagram

Answer:

Tri-State Buffers

Tri-State Buffer is a NOT gate with a control line that disconnects the output from the input. When the control line is high the buffer operates like a NOT gate and when the control line is low the output is disconnected from the output and high impedance is seen at the output. Tri-state buffers are used to disconnect the outputs of devices which are connected or share a common output line. Figure 20.9

Figure 20.9a Tri-State Buffer

Question No: 23 (Marks: 5)

Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram

Answer:

Operation of Odd-Parity Generator Circuit

The timing diagram shows the operation of the Odd-Parity generator circuit. Figure 14.3.
The A, B, C and D timing diagrams represent the changing 4-bit data values. During time interval t0 the 4-bit data value is 0000, during time interval t1, the data value changes to
0001.
Similarly during time intervals t2, t3, t4 up to t8 the data values change to 0010, 0011, 0100 and 1000 respectively. During interval t0 the output of the two XOR gates is 0 and
0, therefore the output of the XNOR gate is 1. At interval t1, the outputs of the two XOR gates is 1 and 0, therefore the output of the XNOR gate is 0. The output P can similarly be traced for intervals t2 to t8.

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Paper # 2

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

Question No: 1 (Marks: 1) - Please choose one

In the binary number "10011" the weight of the most significant digit is _____

- ► 2^4 (2 raise to power 4)
- ► 2^3 (2 raise to power 3)
- ► 2^0 (2 raise to power 0)
- ► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) - Please choose one

An S-R latch can be implemented by using _____ gates

- ► AND, OR
- ► NAND, NOR
- ► NAND, XOR
- ► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one

A latch has _____ stable states

- ► One
- ► Two
- ► Three
- ► Four

Question No: 4 (Marks: 1) - Please choose one

Sequential circuits have storage elements

► True

► False

Question No: 5 (Marks: 1) - Please choose one

The ABEL symbol for "XOR" operation is

► $

► #

► !

► &

Question No: 6 (Marks: 1) - Please choose one

A Demultiplexer is not available commercially.

► True

► False

Question No: 7 (Marks: 1) - Please choose one

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► A parallel to serial converter circuit

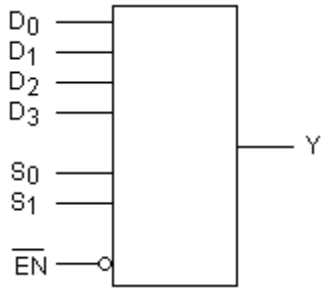
► A counter circuit

► A BCD to Decimal decoder

► A 2-to-8 bit decoder

Question No: 8 (Marks: 1) - Please choose one

The device shown here is most likely a



► Comparator

► **Multiplexer**

► Demultiplexer

► Parity generator

Question No: 9 (Marks: 1) - Please choose one

The main use of the Multiplexer is to

► **Select data from multiple sources and to route it to a single Destination**

► Select data from Single source and to route it to a multiple Destinations

► Select data from Single source and to route to single destination

► Select data from multiple sources and to route to multiple destinations

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters

► three AND gates, two OR gates, one inverter

► **two AND gates, one OR gate, two inverters**

► two AND gates, one OR gate

Question No: 11 (Marks: 1) - Please choose one

The binary value of 1010 is converted to the product term $\bar{A}B\bar{C}D$

► True

► False

Question No: 12 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4

► 8

► 12

► 16

Question No: 13 (Marks: 1) - Please choose one

Following is standard POS expression

$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$

► True

► False

Question No: 14 (Marks: 1) - Please choose one

The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined

► One

► Zero

► 10 (binary)

Question No: 15 (Marks: 1) - Please choose one

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit

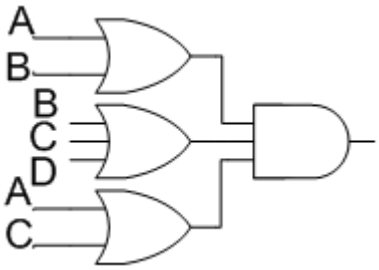
► 7-bit

► 8-bit

► 16-bit

Question No: 16 (Marks: 1) - Please choose one

The diagram given below represents _____



► Demorgans law

► Associative law

► Product of sum form

► Sum of product form

Question No: 17 (Marks: 1)

How can a PLD be programmed?

Answer:

PLDs are programmed with the help of computer which runs the programming software. The computer is connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

Question No: 18 (Marks: 1)

How many input and output bits do a Half-Adder contain?

Answer:

The Half-Adder has a 2-bit input and a 2-bit output.

Question No: 19 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?

Answer:

The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder described earlier figure 16.9. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure

Question No: 20 (Marks: 3)

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.

Answer:

Device declaration, pin declarations and set declarations.

Question No: 21 (Marks: 5)

Explain with example how noise affects Operation of a CMOS AND Gate circuit.

Answer:

Two CMOS 5 volt series AND gates are connected together. Figure 7.3 The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid VOH range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

Question No: 22 (Marks: 10)

explain the SOP based implementation of the Adjacent 1s Detector Circuit:

Answer:

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in the input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111 the output function is a 1. Implementing the circuit directly from the function table based on the SOP form requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3.

The total gate count is

- One 8 input OR gate
- Eight 4 input AND gates
- Ten NOT gates

The expression can be simplified using a Karnaugh map, figure 13.4, and then the simplified expression can be implemented to reduce the gate count. The simplified expression

isAB + CD +BC . The circuit implemented using the expression AB + CD +BC has reduced to 3 input OR gate and 2 input AND gates.
The simplified Adjacent 1s Detector circuit uses only four gates reducing the cost, the size of the circuit and the power requirement. The propagation delay of the circuit is of the order of two gates

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Paper # 3

MIDTERM EXAMINATION

Fall 2009

CS302- Digital Logic Design (Session - 5)

Ref No: 1022709

Time: 60 min

Marks: 38

Question No: 1 (Marks: 1) - Please choose one

According to Demorgan's theorem:

$\overline{A+B+C}$ = _____

- A.B.C
- $A+\overline{B.C}$
- $\overline{A}.\overline{B}.\overline{C}$
- $\overline{A.B}+C$

Question No: 2 (Marks: 1) - Please choose one

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

- 2-bit
- 7-bit
- **8-bit**
- 16-bit

Question No: 3 (Marks: 1) - Please choose one

The AND Gate performs a logical _____function

- Addition
- Subtraction
- **Multiplication**
- Division

Question No: 4 (Marks: 1) - Please choose one

NOR gate is formed by connecting _____

- ► OR Gate and then NOT Gate
- ► NOT Gate and then OR Gate
- ► AND Gate and then OR Gate page50
- ► OR Gate and then AND Gate

Question No: 5 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

- ► TTL
- ► CMOS 3.5 series
- ► CMOS 5 Series
- ► Power dissipation of all circuits increases with time.

Question No: 6 (Marks: 1) - Please choose one

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

- ► True
- ► False

Question No: 7 (Marks: 1) - Please choose one

When the control line in tri-state buffer is high the buffer operates like a _____ gate

- ▶ AND
- ▶ OR
- ▶ NOT
- ▶ XOR

Question No: 8 (Marks: 1) - Please choose one

The GAL22V10 has _____ inputs

- ▶ 22
- ▶ 10
- ▶ 44
- ▶ 20

Question No: 9 (Marks: 1) - Please choose one

The ABEL symbol for "OR" operation is

- ▶ !
- ▶ &
- ▶ #
- ▶ $

Logic Operation ABEL Symbol

NOT	!
AND	&
OR	#
XOR	$

Question No: 10 (Marks: 1) - Please choose one

The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements**
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) - Please choose one

All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon)**
► " endl " (keyword "endl")

Question No: 12 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

► **4**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one

"Sum-of-Weights" method is used _____

► **to convert from one number system to other**
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14 (Marks: 1) - Please choose one

Circuits having a bubble at their outputs are considered to have an active-low output.

► **True**

► False

Question No: 15 (Marks: 1) - Please choose one

$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of _____

► **Product of sum form**

► Sum of product form

► Demorgans law

► Associative law

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

► **Power consumption of TTL is higher than of CMOS**

► Power consumption of CMOS is higher than of TTL

► Both TTL and CMOS have same power consumption

► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Question No: 17 (Marks: 1)

Which device performs an operation which is the opposite of the Decoder function?

Answer:

Encoder function.

Question No: 18 (Marks: 1)

Name any two modes in which PALs are programmed.

Answer:

PAL devices are programmed by blowing the fuses permanently using over voltage.

Question No: 19 (Marks: 2)

Explain Combinational Function Devices?

Ans;

Xor, Xnor, NAND, NOR are combinational function devices.

Question No: 20 (Marks: 3)

Differentiate between hexadecimal and octal number system

Answer:

Octal - base 8

Hexadecimal - base 16

Octal and hex are used to represent numbers instead of decimal because there is a very easy and direct way to convert from the "real" way that computers store numbers (binary) to something easier for humans to handle (fewer symbols). To translate a binary number to octal, simply group the binary digits three at a time and convert each group. For hex, group the binary digits four at a time.

Question No: 21 (Marks: 5)

Explain "Sum-of-Weights Method" for Hexadecimal to Decimal Conversion with at least one example ?

Answer:

The hexadecimal (Hex) numbering system provides even shorter notation than octal. Hexadecimal uses a base of 16. It employs 16 digits: number 0 through 9, and letters A through F, with A through F substituted for numbers 10 to 15, respectively, Hexadecimal numbers can be expressed as their decimal equivalents by using the sum of weights method, as shown in the following example:

Weight	2	1	0	
Hex. Number	1	B	7	
				$7 \times 16^0 = 7 \times 1 = 7$
				$11 \times 16^1 = 11 \times 16 = 176$
				$1 \times 16^2 = 1 \times 256 = 256$
			Sum of products	439_{10}

Like octal numbers, hexadecimal numbers can easily be converted to binary or vise versa. Conversion is accomplished by writing the 4-bit binary equivalent of the hex digit for each position, as illustrated in the following example:

Hex. Number 1 B 7



Binary number

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7

8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Question No: 22 (Marks: 10)

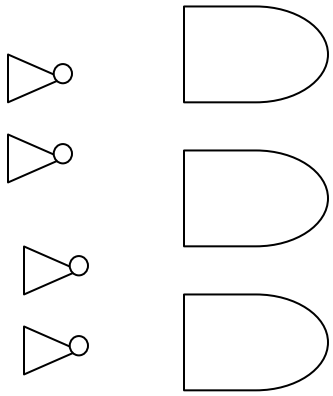
Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression for (A > B)

Ans:

X_1	X_0	Y_1	Y_0	X<Y	X=Y	X>Y
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1

1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

.



The circuit has inputs X_1X_0 and Y_1Y_0 and outputs X > Y, the expression for > is $X_1\overline{Y_1} + X_0\overline{Y_1}\,\overline{Y_0} + X_1X_0\overline{Y_0}$
time is out……

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MIDTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design (Session - 6)
Ref No: 1351363
Time: 60 min
Marks: 38

Question No: 1 (Marks: 1) - Please choose one

The maximum number that can be represented using unsigned octal system is _____

- ► 1
- ► 7
- ► 9
- ► 16

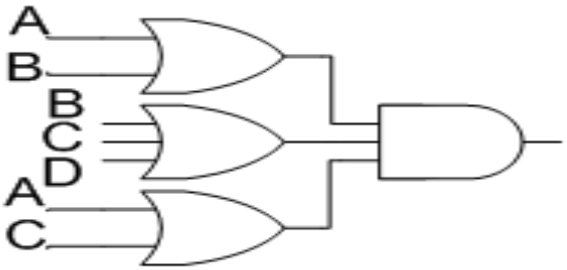
Question No: 2 (Marks: 1) - Please choose one

If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

- ► 0
- ► 1
- ► 2
- ► 3

Question No: 3 (Marks: 1) - Please choose one

The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► Sum of product form

Question No: 4 (Marks: 1) - Please choose one

The range of Excess-8 code is from _____ to _____

► +7 to -8

► +8 to -7

► +9 to -8

► -9 to +8

Question No: 5 (Marks: 1) - Please choose one

A non-standard POS is converted into a standard POS by using the rule _____

► $A+\overline{A}=1$

► $A\overline{A}=0$

► $1+A=1$

► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4

► 8

► 12

► 16

Question No: 7 (Marks: 1) - Please choose one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1

- A > B = 0, A < B = 1, A = B = 0
- **A > B = 1, A < B = 0, A = B = 0**
- A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one

A particular Full Adder has

- **3 inputs and 2 output**
- 3 inputs and 3 output
- 2 inputs and 3 output
- 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one

The function to be performed by the processor is selected by set of inputs known as _ _ _ _ _ _ _ _

- ***Function Select Inputs***
- MicroOperation selectors
- OPCODE Selectors
- None of given option

Question No: 10 (Marks: 1) - Please choose one

For a 3-to-8 decoder how many 2-to-4 decoders will be required?

- **2**
- 1
- 3

► 4

Question No: 11 (Marks: 1) - Please choose one

GAL is an acronym for _____.

► Giant Array Logic
► General Array Logic
► **Generic Array Logic** page183
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

► **4**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one

A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law**

Question No: 14 (Marks: 1) - Please choose one

2's complement of any binary number can be calculated by

► adding 1's complement twice
► adding 1 to 1's complement
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting most significant bit

Question No: 15 (Marks: 1) - Please choose one

The binary value "1010110" is equivalent to decimal _____

► 86
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one

Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► XOR

Question No: 17 (Marks: 2)

For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination.

$$\overline{A.\bar{B} + \bar{A}.\bar{B}.C.D}$$

Ans:

The Multiplexers are used to route the contents of any two registers to the ALU inputs.

Many Audio signals in telephone network.

Computer use Dynamic Memory addressing using same address line for row and column addressing to access data.

Question No: 18 (Marks: 2)

Provide some of the inputs for which the adjacent 1s detector circuit have active high output?

Ans:

The Adjacent 1s Detector accepts 4-bit inputs.

If two adjacent 1s are detected in the input, the output is set to high.

input combinations will be

1. **0011,**
2. **0110,**
3. **0111,**
4. **1011,**
5. **1100,**
6. **1101,**
7. **1110 and**
8. **1111**

the output function is a 1.

Question No: 19 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

S	R	Action
0	0	Keep state
0	1	Q=0
1	0	Q=1
1	1	Restricted combination

Question No: 20 (Marks: 3)

For a two bit comparator circuit specify the inputs for which A > B

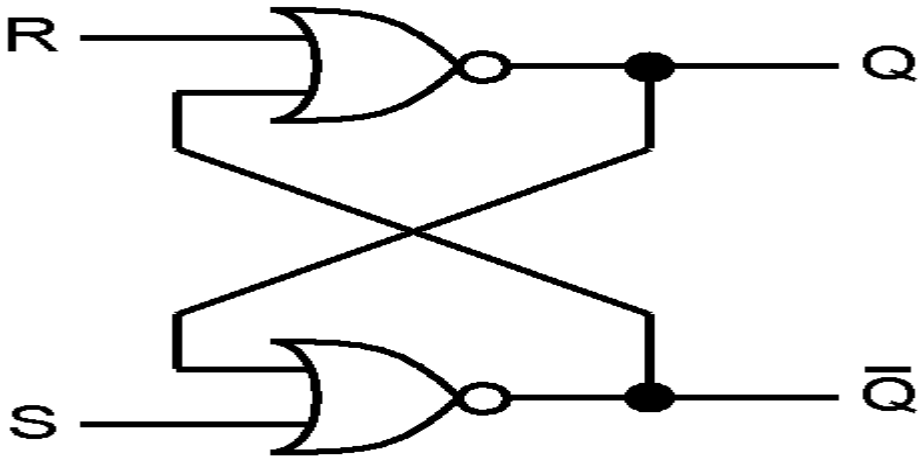
Ans:

1. 01 00,
2. 10 00,
3. 10 01,
4. 11 00,
5. 11 01 and
6. 11 10

Question No: 21 (Marks: 3)

Draw the circuit diagram of NOR based S-R Latch ?

Ans:



Question No: 22 (Marks: 5)

One of the ABEL entry methods uses logic equations; explain it with at least a single example.

Ans:

In ABEL any letter or combination of letters and numbers can be used to identify variables.
ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'.

All ABEL equations must end with ';'

Boolean expression F = AB' + AC + (BD)' is written in ABEL as F = A &! B # A & C #! B & !D;

Question No: 23 (Marks: 5)

Explain Carry propagation in Parallel binary adder?

Ans:

Parallel binary adder:

A binary adder circuit is described using dynamic transistor logic in which for high speed carry propagation the adder stages are grouped in pairs or larger numbers and additional dynamic logic means is provided in each group to control a single transistor connected in series in the carry propagation path over the group.

The transistors used in the specific embodiments are MOS transistors, but some or all of these could be replaced by junction FET's or bipolar transistors.

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Hackers Group
Mandi Bahauddin
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Hearthacker124@gmail.com

Paper # 4

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

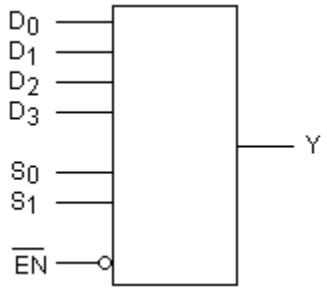
Question No: 1 (Marks: 1) - Please choose one

GAL can be reprogrammed because instead of fuses _____ logic is used in it

- ► E^2CMOS
- ► TTL
- ► CMOS+
- ► None of the given options

Question No: 2 (Marks: 1) - Please choose one

The device shown here is most likely a



- ► Comparator
- ► **Multiplexer**
- ► Demultiplexer
- ► Parity generator

Question No: 3 (Marks: 1) - Please choose one

If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated?

► 2^{nd}
► 4^{th}
► 14^{th}
► No output wire will be activated

Question No: 4 (Marks: 1) - Please choose one

Half-Adder Logic circuit contains 2 XOR Gates

► True
► False

Question No: 5 (Marks: 1) - Please choose one

A particular Full Adder has

► 3 inputs and 2 output
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 6 (Marks: 1) - Please choose one

$Sum = A \oplus B \oplus C$

$CarryOut = C(A \oplus B) + AB$ are the Sum and CarryOut expression of

► Half Adder
► Full Adder
► 3-bit parralel adder
► MSI adder cicuit

Question No: 7 (Marks: 1) - Please choose one

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► True
► False

Question No: 8 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10

Here output combination should A < B

Question No: 9 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► 16

Question No: 10 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► TTL
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 11 (Marks: 1) - Please choose one

The decimal "8" is represented as _____ using Gray-Code.

► 0011
► 1100
► 1000
► 1010

Question No: 12 (Marks: 1) - Please choose one

(A+B).(A+C) = _____

► B+C
► A+BC
► AB+C
► AC+B

Question No: 13 (Marks: 1) - Please choose one

A.(B + C) = A.B + A.C is the expression of _____

► Demorgan's Law
► Commutative Law
► Distributive Law
► Associative Law

Question No: 14 (Marks: 1) - Please choose one

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► FALSE
► TRUE

Question No: 15 (Marks: 1) - Please choose one

In ANSI/IEEE Standard 754 "Mantissa" is represented by ___-bits_____ bits

► 8-bits
► 16-bits
► 32-bits
► 64-bits

Question No: 16 (Marks: 1) - Please choose one

Caveman number system is Base _____ number system

► 2
► 5
► 10
► 16

Question No: 17 (Marks: 1)

Briefly state the basic principle of **Repeated Multiplication-by-2** Method.

Ans:

Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.

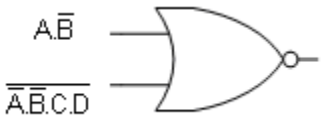
Question No: 18 (Marks: 1)

How standard Boolean expressions can be converted into truth table format.

Ans:

Standard Boolean expressions can be converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Question No: 19 (Marks: 2)



What will be the out put of the diagram given below

A.B + A.B.C.D

Question No: 20 (Marks: 3)

When an Input (source) file is created in ABEL a module is created which has three sections. Name These three sections.

Answer:

The three sections are:

- Boolean Equations
- Truth Tables
- State Diagrams

Question No: 21 (Marks: 5)

Explain "AND" Gate and some of its uses :

Answer:

AND gates are used to combine multiple signals, if all the signals are TRUE then the output will also be TRUE. If any of the signals are FALSE, then the output will be false. ANDs aren't used as much as NAND gates; NAND gates use less components and have the advantage that they be used as an inverter.

Question No: 22 (Marks: 10)

Write down different situations where we need the sequential circuits.

Answer:

Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.

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Hearthacker124@gmail.com

Paper # 7

MIDTERM EXAMINATION
Fall 2009
CS302- Digital Logic Design (Session - 2)

Time: 60 min
Marks: 38

Student Info	
StudentID:	
Center:	OPKST
ExamDate:	12/7/2009 12:00:00 AM

For Teacher's Use Only									
Q No.	1	2	3	4	5	6	7	8	Total
Marks									
Q No.	9	10	11	12	13	14	15	16	
Marks									
Q No.	17	18	19	20	21	22			
Marks									

Question No: 1 (Marks: 1) - Please choose one

Which of the number is not a representative of hexadecimal system

- ► 1234
- ► ABCD
- ► 1001
- ► DEFH

Question No: 2 (Marks: 1) - Please choose one

The Unsigned Binary representation can only represent positive binary numbers

- ► True
- ► False

Question No: 3 (Marks: 1) - Please choose one

The values that exceed the specified range can not be correctly represented and are considered as _____

- ► Overflow page23
- ► Carry
- ► Parity
- ► Sign value

Question No: 4 (Marks: 1) - Please choose one

The 4-bit 2's complement representation of "-7" is _____

- ► 0111
- ► 1111

► 1001

► 0110

L-2

Question No: 5 (Marks: 1) - Please choose one

$\overline{A}B + \overline{A}B\overline{C} + AC$ is an example of _____

► Product of sum form

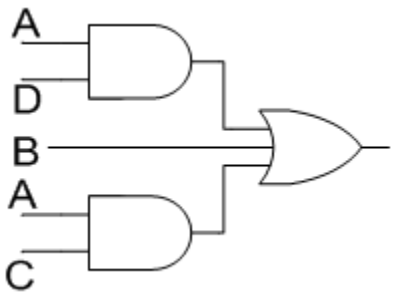
► Sum of product form

► Demorgans law

► Associative law

Question No: 6 (Marks: 1) - Please choose one

The diagram given below represents _____



► Demorgans law

► Associative law

► Product of sum form

► Sum of product form

Question No: 7 (Marks: 1) - Please choose one

The output of an AND gate is one when _____

► All of the inputs are one

► Any of the input is one

► Any of the input is zero

► All the inputs are zero

Question No: 8 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► 16

Question No: 9 (Marks: 1) - Please choose one

A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► 4 inputs and 7 outputs
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

Question No: 10 (Marks: 1) - Please choose one

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► 2-input, 4-bit

Question No: 11 (Marks: 1) - Please choose one

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

► AND
► OR
► NOT
► XOR

Question No: 12 (Marks: 1) - Please choose one

In ABEL the variable 'A' is treated separately from variable 'a'

► True
► False

Question No: 13 (Marks: 1) - Please choose one

The ABEL notation equivalent to Boolean expression A+B is:

► A & B
► A ! B
► A # B
► A $ B

L-21

Question No: 14 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET
► RESET
► Clear
► Invalid

Question No: 15 (Marks: 1) - Please choose one

Demultiplexer has

- ► Single input and single outputs.
- ► Multiple inputs and multiple outputs.
- ► **Single input and multiple outputs.**
- ► Multiple inputs and single output.

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

- ► **Power consumption of TTL is higher than of CMOS**
- ► Power consumption of CMOS is higher than of TTL
- ► Both TTL and CMOS have same power consumption
- ► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Question No: 17 (Marks: 1)

Briefly state the basic principle of **Repeated Division-by-2** method.

Repeated Division-by-2

Repeated Division-by-2 method allows decimal numbers of any magnitude to be converted into binary. In this method the Decimal number to be converted into its Binary equivalent is repeatedly divided by 2. The divisor is selected as 2 because the decimal number is being converted into Binary a Base-2 Number system. Repeated division method can be used to convert decimal number into any Number system by repeated division by the Base-Number. For example, the decimal number can be converted into the Caveman Number system by repeatedly dividing by 5, the Base number of the Caveman Number System. The Repeated

Division method will be used in latter lectures to convert decimal into Hexadecimal and Octal Number Systems.
In the Repeated-Division method the Decimal number to be converted is divided by the Base Number, in this particular case 2. A quotient value and a remainder value is generated, both values are noted done. The remainder value in all subsequent divisions would be either a 0 or a 1. The quotient value obtained as a result of division by 2 is divided again by 2. The new quotient and remainder values are again noted down. In each step of the repeated division method the remainder values are noted down and the quotient values are repeatedly divided by the base number. The process of repeated division stops when the quotient value becomes zero. The remainders that have been noted in consecutive steps are written out to indicate the Binary equivalent of the Original Decimal Number.

Question No: 18 (Marks: 1)

Briefly state the basic principle of **Repeated Multiplication-by-2** Method.

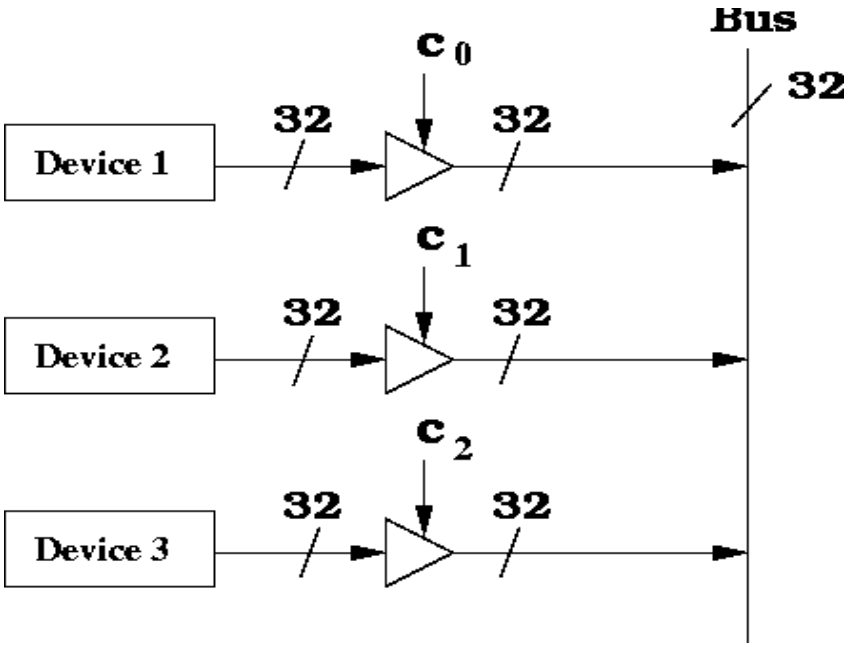
Repeated Multiplication-by-2 Method
An alternate to the Sum-of-Weights method used to convert Decimal fractions to equivalent Binary fractions is the repeated multiplication by 2 methods. In this method the number to be converted is repeatedly multiplied by the Base Number to which the number is being converted to, in this case 2. A new number having an Integer part and a
Fraction part is generated after each multiplication. The Integer part is noted down and the fraction part is again multiplied with the Base number 2. The process is repeated until the fraction term becomes equal to zero.
Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary. The conversion of Decimal fraction 0.625 into Binary equivalent using the

Repeated Multiplication-by-2 method is illustrated in a tabular form.

Table 2.4. Reading the Integer column from bottom to top and placing a decimal point in the left most position gives 0.101 the binary equivalent of decimal fraction 0.625

Question No: 19 (Marks: 2)

Draw the circuit diagram of a Tri-State buffer.



Question No: 20 (Marks: 3)

Add -13 and +7 by converting them in binary system your result must be in binary.

Question No: 21 (Marks: 5)

Explain "Sum of Weights" method with example for "Octal to Decimal" conversion

1. Sum-of-Weights Method

Sum-of-weights as the name indicates sums the weights of the Binary Digits (bits) of a Binary Number which is to be

represented in Decimal. The Sum-of-Weights method can be used to convert a Binary number of any magnitudes to its equivalent Decimal representation.

In the Sum-of-Weights method an extended expression is written in terms of the Binary Base Number 2 and the weights of the Binary number to be converted. The weights correspond to each of the binary bits which are multiplied by the corresponding binary value. Binary bits having the value 0 do not contribute any value towards the final sum expression.

The Binary number 101102 is therefore written in the form of an expression having weights $2^0, 2^1, 2^2, 2^3$ AND 2^4 corresponding to the bits 0, 1, 1, 0 and 1 respectively.

Weights 2^0 AND 2^3 do not contribute in the final sum as the binary bits corresponding to these weights have the value 0.

$10110_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$= 16 + 0 + 4 + 2 + 0$

$= 22$

Question No: 22 (Marks: 10)

Explain the Implementation of an Odd-Parity Generator Circuit i.e by drawing function table, maping it to K-map and then simplifying the expression.

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Mandi Bahauddin
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Hearthacker124@gmail.com

Current paper subjective question:

Was my CS302_DLD paper. Total 23 questions out of which 16 MCQ's.

2 questions of two marks each were from the topic Adder.
A boolian expression wes given and had to find a logic 1 for it.
One 5 marks question from parity method.

2day was my 2nd paper of cs302
this was my papers

SOP to POS conversion 3mark
S-R latch Diagram 5mark
Nor gate table 3mark

8 t0 3 bit encoder 5mark
Tri-stuff diagram 3mark

mcqz zyda tar start lec mn say aye thay
binary additin
2's complemnt
k-map

Assalam o Alaikum

Today I attempted CS302 paper

Paper was of 38 marks.
16 MCQs and 22 marks paper comprised of long questions.
2 marks question was "Write the uses of multiplexer".

2 marks question was "Write any two advantages of boolean expressions".

2 marks question was "Draw the diagram of odd parity generator circuit".

3 marks question was "What does a 8-bit adder/subtracter circuit do"?

3 marks question was "Draw the function table of 3 to 8 decoder".
5 marks question was "Describe 16 bit ALU".

5 marks question was "Describe in your own words about latches".

CS302 CURRENT MIDTERM PAPER

What is the role of MOS transistor in Mask ROM?

How many input and output bits do a Half-Adder contain?

How can a PLD be programmed?

DRAW THE CIRCUIT DIAGRAM OF GATED S-R LATCH.?

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL?

Explain with example how noise affects Operation of a CMOS AND Gate circuit?

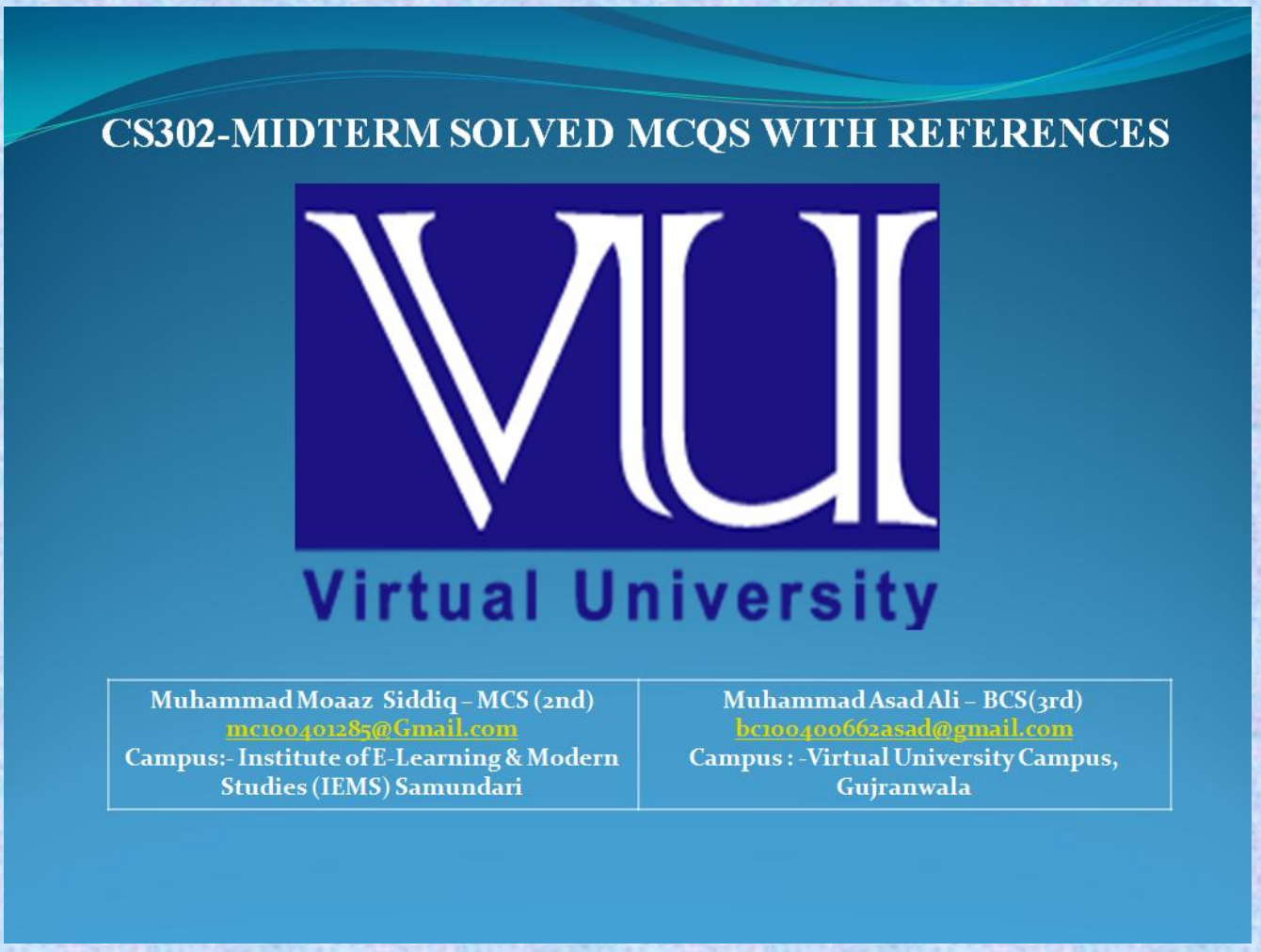
GIVEN THE FOLLOWING STATEMENT USED IN PLD PROGRAMMING:
Y PIN 23 ISTYPE 'COM';
Explain what does this statement mean?

VARIABLE Y AT OUTPUT PIN 23 WHICH IS A COMBINATIONAL OUTPUT AVAILABLE DIRECTLY FROM THE AND-OR GATE ARRAY OUTPUT.

Y = VARIABLE Y
PIN 23 = PIN NUMBER 23
ISTYPE "COM" = OUTPUT TYPE COMBINATIONAL

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Muhammad Moaaz Siddiq – MCS (2nd) mc100401285@Gmail.com Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari	Muhammad Asad Ali – BCS(3rd) bc100400662asad@gmail.com Campus : -Virtual University Campus, Gujranwala

MIDTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► When one or more product terms in the expression are equal to 1. (Page 86)

Question No: 2 (Marks: 1) - Please choose one
The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10 (Page 109)

Question No: 3 (Marks: 1) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► True (Page 154)
► False

Question No: 4 (Marks: 1) - Please choose one
High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► 0.9 V (Page 65)
► 3.3 V

Question No: 5 (Marks: 1) - Please choose one
If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582 (But not sure)
► 2.4582
► 24582
► 0.24582

Question No: 6 (Marks: 1) - Please choose one

The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

- ► Undefined
- ► **One**
- ► Zero
- ► 10 (binary)

Question No: 7 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

- ► **SET (page 220)**
- ► RESET
- ► Clear
- ► Invalid

Question No: 8 (Marks: 1) - Please choose one

3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

- ► Low switching speeds, high power dissipation
- ► Fast switching speeds, high power dissipation
- ► **Fast switching speeds, very low power dissipation (page61)**
- ► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) - Please choose one

The binary value "1010110" is equivalent to decimal _____

- ► **86 (According to Formula)**
- ► 87
- ► 88
- ► 89

Question No: 10 (Marks: 1) - Please choose one

The _____ Encoder is used as a keypad encoder.

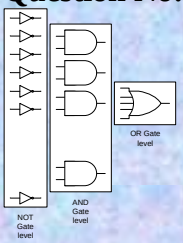
- ► 2-to-8 encoder
- ► 4-to-16 encoder
- ► BCD-to-Decimal
- ► **Decimal-to-BCD Priority (Page 166)**

Question No: 11 (Marks: 1) - Please choose one

How many data select lines are required for selecting eight inputs?

- ► 1
- ► 2
- ► **3 click here for detail**
- ► 4

Question No: 12 (Marks: 1) - Please choose one



the diagram above shows the general implementation of _____ form

- ► boolean
- ► arbitrary
- ► POS
- ► **SOP**

Question No: 13 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

- ► **4 (Page 217)**
- ► 8
- ► 12
- ► 16

Question No: 14 (Marks: 1) - Please choose one

Demultiplexer has

- ► Single input and single outputs.
- ► Multiple inputs and multiple outputs.
- ► **Single input and multiple outputs. (Page 178)**
- ► Multiple inputs and single output.

Question No: 15 (Marks: 1) - Please choose one

The expression _____ is an example of Commutative Law for Multiplication.

- ► AB+C = A+BC
- ► A(B+C) = B(A+C)
- ► **AB=BA (Page 72)**
- ► A+B=B+A

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

Question No: 16 (Marks: 1) - Please choose one
"Sum-of-Weights" method is used _____

► **to convert from one number system to other (Page 14)**
► to encode data
► to decode data
► to convert from serial to parralel data

MIDTERM EXAMINATION
Spring 2010

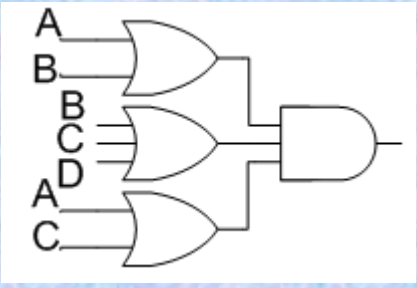
Question No: 1 (Marks: 1) - Please choose one
The maximum number that can be represented using unsigned octal system is _____

► 1
► **7 (Page 31)**
► 9
► 16

Question No: 2 (Marks: 1) - Please choose one
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► **2 (Page 26)**
► 3

Question No: 3 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form (According to rule of theorem)**
► Sum of product form

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

Question No: 4 (Marks: 1) - Please choose one
The range of Excess-8 code is from _____ to _____

► **+7 to -8 (Page 34)**
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____

► $A+\overline{A}=1$
► $A\overline{A} = 0$ **(Page 85)**
► $1+A=1$
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8 (Page 89)**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► **A > B = 1, A < B = 0, A < B = 1**
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one
A particular Full Adder has

► **3 inputs and 2 output (Page 135)**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as _____

► **Function Select Inputs (Page 147)**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement (Page 144)**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR (Page 186)**

MIDTERM EXAMINATION 2010

1. **The binary value "11011" is equivalent to _____**

►**1B (According to rule)**
►1C
►1D
►1E

2. **An important application of AND Gate is its use in counter circuit**

►**True (Page 281)**
►False

3. **The OR Gate performs a Boolean _____ function**

►**Addition (Page 42)**
►Subtraction
►Multiplication
►Division

4. **TTL based devices work with a dc supply of ____ Volts**

►+10
►**+5 (Page 61)**
►+3
►3.3

5. **A standard POS form has _____ terms that have all the variables in the domain of the expression.**

►**Sum (Page 85)**
►Product
►Min
►Composite

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

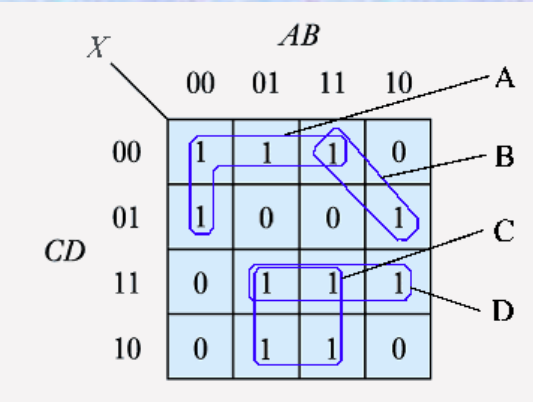
Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

6. **A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.**

►2
►4
►**8 (According to rule)**
►16

7. **A BCD to 7-Segment decoder has**

►3 inputs and 7 outputs
►**4 inputs and 7 outputs (Page 103)**
►7 inputs and 3 outputs
► inputs and 4 outputs



8. **In the Karnaugh map shown above, which of the loops shown represents a legal grouping?**

►A
►
►**C click here for detail**
►D

9. **The binary value of 1010 is converted to the product term** $\bar{A}B\bar{C}D$

►True
►**False**

10. **The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?**

►A > B = 1, A < B = 0, A < B = 1
►A > B = 0, A < B = 1, A = B = 0
►**A > B = 1, A < B = 0, A = B = 0 (Page 109)**
►A > B = 0, A < B = 1, A = B = 1

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

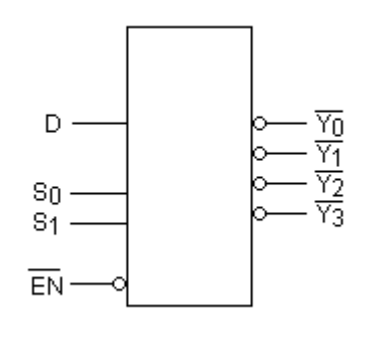
11. $C_{out1} + S_3(S_2 + S_1)$ **is boolean expression for**

►Half Adder
►Full Adder
►**The Invalid BCD Detector Circuit (page 142)**
►Parity Checker

12. 3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

►**True (Page 160)**
►False

13. The device shown here is most likely a _____



►Comparator
►Multiplexer
►**Demultiplexer click here for detail**
►Parity generator

14. The GAL22V10 has ____ inputs

►**22 (Page 195)**
►10
►44
►20

15. A latch retains the state unless

►Power is turned off
►**Input is changed (page 218)**
►Output is changed
►Clock pulse is changed

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

16. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

►**SET (Page 220)**
►RESET
►Clear
►Invalid

17. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (V_{oH}) will be in the range of _____ volts.

►4 to 4.5
►**4.5 to 5**
►0 to 4.5
►0 to 3.5

18. A.(B.C) = (A.B).C is an expression of _____

►Demorgan's Law
►Distributive Law
►Commutative Law
►**Associative Law (Page 72)**

19. The 4-bit 2's complement representation of "+5" is _____

►1010
►1110
►**1011**
►0101

20. Which of the number is not a representative of hexadecimal system

►1234
►ABCD
►1001
►**DEHF Hexa does not have H as remainder**

MIDTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one

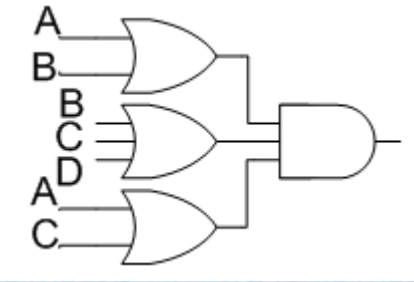
► 1
► **7**
► 9
► 16

Muhammad Moaaz Siddiq – MCS (2nd)	Muhammad Asad Ali – BCS(3rd)
mc100401285@Gmail.com	bc100400662asad@gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari	Campus : -Virtual University Campus, Gujranwala

Question No: 2 (Marks: 1) - Please choose one
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

- ► 0
- ► 1
- ► **2 (Page 26)**
- ► 3

Question No: 3 (Marks: 1) - Please choose one
The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► **Product of sum form (According to rule)**
- ► Sum of product form

Question No: 4 (Marks: 1) - Please choose one
The range of Excess-8 code is from _____ to _____

- ► **+7 to -8 (Page 34)**
- ► +8 to -7
- ► +9 to -8
- ► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____

- ► $A+\overline{A}=1$
- ► $A\overline{A}=0$ **(Page 85)**
- ► $1+A=1$
- ► A+B = B+A

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8 (Page 89)**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one
A particular Full Adder has
► **3 inputs and 2 output (Page 135)**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as ____

► **Function Select Inputs (Page 147)**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► **16**

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement (Page 144)**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal ____ _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► **NOT (page 196)**
► **XOR**

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

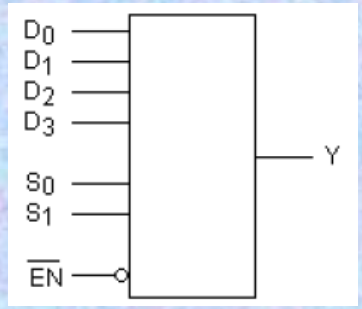
Question No: 1 (Marks: 1) - Please choose one

GALcan be reprogrammed because instead of fuses _____logic is used in it

- ► **E^2CMOS (Page 191)**
- ► TTL
- ► CMOS+
- ► **None of the given options**

Question No: 2 (Marks: 1) - Please choose one

The device shown here is most likely a



- ► Comparator
- ► **Multiplexer click here for detail**
- ► Demultiplexer
- ► Parity generator

Question No: 3 (Marks: 1) - Please choose one

If"1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

- ► 2^{nd}
- ► 4^{th}
- ► 14^{th}
- ► **No output wire will be activated (Page 163)**

Question No: 4 (Marks: 1) - Please choose one

Half-Adder Logic circuit contains 2 XOR Gates

- ► True
- ► **False (Page 135)**

Question No: 5 (Marks: 1) - Please choose one

A particular Full Adder has

- ► **3 inputs and 2 output (Page 135)**
- ► 3 inputs and 3 output
- ► 2 inputs and 3 output
- ► **2 inputs and 2 output**

Question No: 6 (Marks: 1) - Please choose one

$Sum = A \oplus B \oplus C$

$CarryOut = C(A \oplus B) + AB$

are the Sum and CarryOut expression of

- ► Half Adder
- ► **Full Adder (Page 135)**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

► 3-bit parralel adder
► MSI adder cicuit

Question No: 7 (Marks: 1) - Please choose one

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True click here for detail**
► **False**

Question No: 8 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► **A=01, B=10 (Page 109)**

Question No: 9 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____cells for min or max terms

► 4
► 8
► 12
► **16 (Page 90)**

Question No: 10 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____devices remains constant throughout their operation.

► **TTL (Page 65)**
► CMOS 3.5 series
► CMOS 5 Series
► **Power dissipation of all circuits increases with time.**

Question No: 11 (Marks: 1) - Please choose one

The ecimal "8" is represented as _____using Gray-Code.

► 0011
► **1100 (page 36)**
► 1000
► 1010

Question No: 12 (Marks: 1) - Please choose one

(A+B).(A+C) = _____

► B+C
► **A+BC (According to rule)**
► AB+C
► AC+B

Question No: 13 (Marks: 1) - Please choose one

A.(B+ C) = A.B + A.C is the expression of _____

- ► Demorgan's Law
- ► Commutative Law
- ► **Distributive Law (Page 73)**
- ► Associative Law

Question No: 14 (Marks: 1) - Please choose one

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

- ► **FALSE**
- ► **TRUE (Page 50)**

Question No: 15 (Marks: 1) - Please choose one

In ANSI/IEEE Standard 754 "Mantissa" is represented by _____32-bits_____bits

- ► 8-bits
- ► 16-bits
- ► **32-bits (Page 24)**
- ► 64-bits

Question No: 16 (Marks: 1) - Please choose one

Caveman number system is Base _5_____number system

- ► 2
- ► **5 (Page 11)**
- ► 10
- ► 16

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one

According to Demorgan's theorem:

$\overline{A + B + C} =$ _____

- ► A.B.C
- ► $A + \overline{B.C}$
- ► $\overline{A}.\overline{B}.\overline{C}$ **(Page 74)**
- ► $\overline{A.B} + C$

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

Question No: 2 (Marks: 1) - Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► **8-bit (Page 38)**
► 16-bit

Question No: 3 (Marks: 1) - Please choose one
The AND Gate performs a logical _____function

► Addition
► Subtraction
► **Multiplication (Page 40)**
► Division

Question No: 4 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____

► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 5 (Marks: 1) - Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL (Page 65)**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 6 (Marks: 1) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True (Page 154)**
► False

Question No: 7 (Marks: 1) - Please choose one
When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► **NOT (Page196)**
► XOR

Question No: 8 (Marks: 1) - Please choose one
The GAL22V10 has ____ inputs

► **22 (Page 195)**
► 10
► 44
► 20

Question No: 9 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is

► !
► &
► **# (Page 201)**
► $

Question No: 10 (Marks: 1) - Please choose one
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements (Page 207)**
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) - Please choose one
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon) (Page 201)**
► " endl " (keyword "endl")

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216) rep**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
"Sum-of-Weights" method is used _____

► **to convert from one number system to other (Page 14)**
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14 (Marks: 1) - Please choose one
Circuits having a bubble at their outputs are considered to have an active-low output.

► **True (Page 128)**
► False

Question No: 15 (Marks: 1) - Please choose one
$(A + B)(A + \overline{B} + C)(\overline{A} + C)$ is an example of _____

► **Product of sum form (According to rule)**
► Sum of product form
► Demorgans law
► Associative law

Question No: 16 (Marks: 1) - Please choose one
Which one is true:

► **Power consumption of TTL is higher than of CMOS (Page 61)**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

MIDTERM EXAMINATION
Spring 2009

Question No: 1 (Marks: 1) - Please choose one
In the binary number "10011" the weight of the most significant digit is ____

► **2^4 (2 raise to power 4) (Page 13)**
► 2^3 (2 raise to power 3)
► 2^0 (2 raise to power 0)
► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) - Please choose one
An S-R latch can be implemented by using _____ gates

► AND, OR
► **NAND, NOR (Page 218-220)**
► NAND, XOR
► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one
A latch has _____ stable states

- ► One
- ► **Two (Page 218)**
- ► Three
- ► Four

Question No: 4 (Marks: 1) - Please choose one
Sequential circuits have storage elements

- ► **True (Page 8)**
- ► False

Question No: 5 (Marks: 1) - Please choose one
The ABEL symbol for "XOR" operation is

- ► **$ (Page 210)**
- ► #
- ► !
- ► &

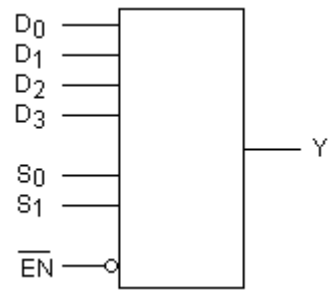
Question No: 6 (Marks: 1) - Please choose one
A Demultiplexer is not available commercially.

- ► **True (Page 178)**
- ► False

Question No: 7 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

- ► **A parallel to serial converter circuit (Page 244)**
- ► A counter circuit
- ► A BCD to Decimal decoder
- ► A 2-to-8 bit decoder

Question No: 8 (Marks: 1) - Please choose one
The device shown here is most likely a



► Comparator
► **Multiplexer click here for detail**
► Demultiplexer
► Parity generator

Question No: 9 (Marks: 1) - Please choose one
The main use of the Multiplexer is to

► **Select data from multiple sources and to route it to a single Destination (Page 167)**
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► **two AND gates, one OR gate, two inverters**
► two AND gates, one OR gate

Question No: 11 (Marks: 1) - Please choose one
The binary value of 1010 is converted to the product term $\overline{A}B\overline{C}D$

► True
► **False**

Question No: 12 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8 (Page 89)**
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
Following is standard POS expression
$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$

► **True (According to logic)**
► False

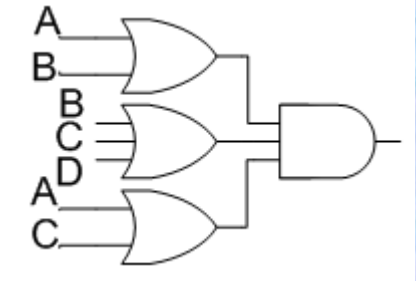
Question No: 14 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined
► **One**
► Zero
► 10 (binary)

Question No: 15 (Marks: 1) - Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► **8-bit (Page 38)**
► 16-bit

Question No: 16 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form (According to rule)**
► Sum of product form

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
Which of the number is not a representative of hexadecimal system

- ► 1234
- ► ABCD
- ► 1001
- ► **DEFH Hexa does not have H as remainder**

Question No: 2 (Marks: 1) - Please choose one
The Unsigned Binary representation can only represent positive binary numbers

- ► **True (Page 21)**
- ► False

Question No: 3 (Marks: 1) - Please choose one
The values that exceed the specified range can not be correctly represented and are considered as _____

- ► **Overflow (Page 23)**
- ► Carry
- ► Parity
- ► Sign value

Question No: 4 (Marks: 1) - Please choose one
The 4-bit 2's complement representation of "-7" is _____

- ► 0111
- ► 1111
- ► **1001 (Page 21)**
- ► 0110

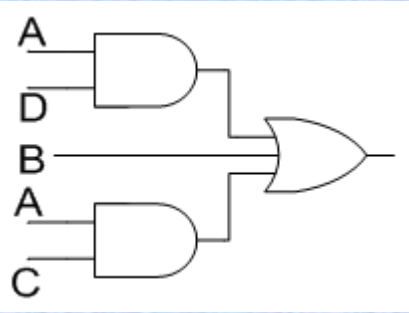
Question No: 5 (Marks: 1) - Please choose one
$\overline{A}B + \overline{A}\overline{B}\overline{C} + AC$ is an example of _____

- ► Product of sum form
- ► **Sum of product form (Page 77)**
- ► Demorgans law
- ► Associative law

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

Question No: 6 (Marks: 1) - Please choose one
The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► **Sum of product form**

Question No: 7 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

- ► **All of the inputs are one**
- ► Any of the input is one
- ► Any of the input is zero
- ► All the inputs are zero

Question No: 8 (Marks: 1) - Please choose one
The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

- ► 4
- ► 8
- ► 12
- ► **16 (Page 90)**

Question No: 9 (Marks: 1) - Please choose one
A BCD to 7-Segment decoder has

- ► 3 inputs and 7 outputs
- ► **4 inputs and 7 outputs (Page 103)**
- ► 7 inputs and 3 outputs
- ► 7 inputs and 4 outputs

Question No: 10 (Marks: 1) - Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

- ► 4-input, 8-bit
- ► 4-input, 16-bit
- ► 2-input, 8-bit
- ► **2-input, 4-bit (Page 169)**

Question No: 11 (Marks: 1) - Please choose one

The PROM
consists of a fixed non-programmable _____ Gate array configured as a decoder.

► **AND (Page 182)**
► OR
► NOT
► XOR

Question No: 12 (Marks: 1) - Please choose one

In ABEL the variable 'A' is treated separately from variable 'a'

► **True (Page 201)**
► False

Question No: 13 (Marks: 1) - Please choose one

The ABEL notation equivalent to Boolean expression A+B is:

► A & B
► A ! B
► **A # B (Page 201)**
► A $ B

L-21

Question No: 14 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► **SET (Page 220)**
► RESET
► Clear
► Invalid

Question No: 15 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs. (Page 178)**
► Multiple inputs and single output.

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

► **Power consumption of TTL is higher than of CMOS (Page 61)**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The first Least Significant digit in decimal number system has

position 0 and weight equal to 1
position 1 and weight equal to 0
position 1 and weight equal to 10
position 0 and weight equal to 10

Question No: 2 (Marks: 1) - Please choose one
The decimal equivalent of the binary number "10011" is

19 (According to rule)
99
29
None of given options

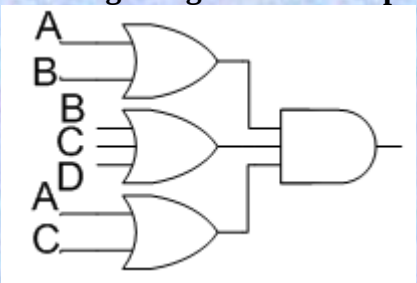
Question No: 3 (Marks: 1) - Please choose one
In ANSI/IEEE Standard 754 "Mantissa" is represented by ____32-bits_____bits

► 8-bits
► 16-bits
► 32-bits (Page 24)
► 64-bits

Question No: 4 (Marks: 1) - Please choose one
The binary value "11011" is equivalent to

1B (According to rule)
1C
1D
1E

Question No: 6 (Marks: 1) - Please choose one
The diagram given below represents



Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

Demorgans law▶
Associative law
Product of sum form (According to rule)
Sum of product form

Question No: 7 (Marks: 1) - Please choose one
NOR gate is formed by connecting

OR Gate and then NOT Gate (Page 47)
NOT Gate and then OR Gate
AND Gate and then OR Gate
OR Gate and then AND Gate

Question No: 8 (Marks: 1) - Please choose one
"74ALS" stands for

Advanced Low-frequency Schottky TTL
Advanced Low-dissipation Schottky TTL
Advanced Low-Power Schottky TTL (Page 61)
Advanced Low-propagation Schottky TTL

Question No: 9 (Marks: 1) - Please choose one
An adder circuit can be used to perform subtraction operation

True (Page 146)
False

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

2 (Page 160)
3
4
1

Question No: 11 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True Page 161
False

Question No: 12 (Marks: 1) - Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a multiplexer.

2-input, 4-bit
4-input, 8-bit
4-input, 16-bit
2-input, 8-bit (Page 171)

Question No: 13 (Marks: 1) - Please choose one
The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected together through a 4-input gate

AND
OR (Page 171-172)
NAND
XOR

Question No: 14 (Marks: 1) - Please choose one
The Programmable Array Logic (PAL) has AND array and a OR array

Fixed, programmable
Programmable, fixed (Page 182)
Fixed, fixed
Programmable, programmable

Question No: 15 (Marks: 1) - Please choose one
Sequential circuits have storage elements

True (Page 218)
False

Question No: 16 (Marks: 1) - Please choose one
Demultiplexer has

Single input and single outputs.
Multiple inputs and multiple outputs.
Single input and multiple outputs. (Page 178)
Multiple inputs and single output.

Proude To Be Virtulian MOAAZ SIDDIQ	**CS302- Digital Logic Design** **SUBJECTIVE SOLVED FROM MIDTERM PAPERS**	**Dec 07,2011**
MC100401285	**MC100401285@gmail.com** **moaaz.pk@gmail.com**	**PSMD01(IEMS)**

CS302-MIDTERM SOLVED SUBJECTIVE WITH REFERENCES

Virtual University

Muhammad Moaaz Siddiq MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

MIDTERM EXAMINATION 2011 (October-November)

Q-21

Draw function table of a half adder circuit? (2)

Answer: - Page 135 Lec14

Half-Adder Logic Circuit

The Half-Adder Logic Circuit can be directly implemented from the Sum and Carry Out Boolean expressions. Figure 14.6

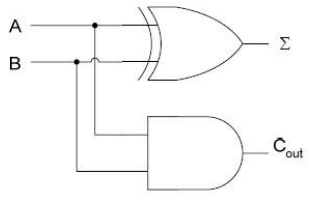


Figure 14.6 Half-Adder Logic Circuit

Q-22

What is difference b/w BCD to decimal decoder and binary 4-to-16 bit decoder? (2)

Answer: (Page 163) Lec17

The operation of the BCD-to-Decimal Decoder is the same as a Binary 4-to-16 decoder, the only difference being that the BCD-to-Decimal Decoder has ten output pins instead of sixteen and the input is a valid BCD number.

Q-23

Explain major use of decoder circuits? (3) Lec16

Answer: (Page 158)

Decoders have two major uses in Computer Systems.

1. Selection of Peripheral Devices

Computers have different internal and external devices like the Hard Disk, CD Drive, Modem, Printer etc. Each of these different devices is selected by specifying different codes. A decoder similar to the Electronic Door Lock/Unlock circuit is used to uniquely select or deselect the appropriate devices.

2. Instruction Decoder

Computer programs are based on instructions which are decode by the Computer Hardware and implemented. These instruction codes are decoded by an Instruction Decoder to generate signals that control different logic circuits like the ALU and memory to perform these operations.

Q-25

PALS comes in different configurations and are identified by a unique number, identify parts of this number? (5)

Answer: (Page 186) Lec19

PALs come in different configurations they are identified by unique number. The numbers begin with the prefix PAL followed by two digits that indicate the number of inputs followed by a letter L active-low, H active-high or P programmable polarity followed by a single or two digits that indicate the number of outputs. In addition to the standard number there may be suffixes which specify the speed, package type and temperature range

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Q-26

One of the ABEL entry methods uses logic equation. Explain at least two examples? (5)

Answer: (Page 201) Lec20

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'. All ABEL equations must end with ';'.

Examples:-

(a) $X = A\bar{B}C + \overline{ABC} + AB + \bar{B}C$

(b) $Y = (\bar{A} + B + \bar{C} + D)(A + B + C)$

Solution

(a)X = A& !B & C # !A & !B & !C # A & B # !B & C;
(b)Y = (!A # B # !C #D) & (A # B # C);

MIDTERM EXAMINATION 2011 (October-November)

Q-21

Draw the function table of 2-to-4 decoder (2 marks)

Answer: (Page 158) Lec16

A 2-to-4 Decoder is represented by the function table.

Input		Output			
I_1	I_0	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Function Table of a 2-to-4 Binary Decoder

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Q-24

Explain BCD to Decimal Decoder (3marks)

Answer: (Page 163) Lec17

"The operation of the BCD-to-Decimal Decoder is the same as a Binary 4-to-16 decoder, the only difference being that the BCD-to-Decimal Decoder has ten output pins instead of sixteen and the input is a valid BCD number. Thus invalid BCD codes 1010, 1011, 1100, 1101, 1110 and 1111 applied at the input of the Decoder do not activate any of the ten outputs."

Q-26

Explain 8-input Multiplexer with the help of circuit Diagram and Function Table. (5marks)

Answer: (Page 170) Lec18

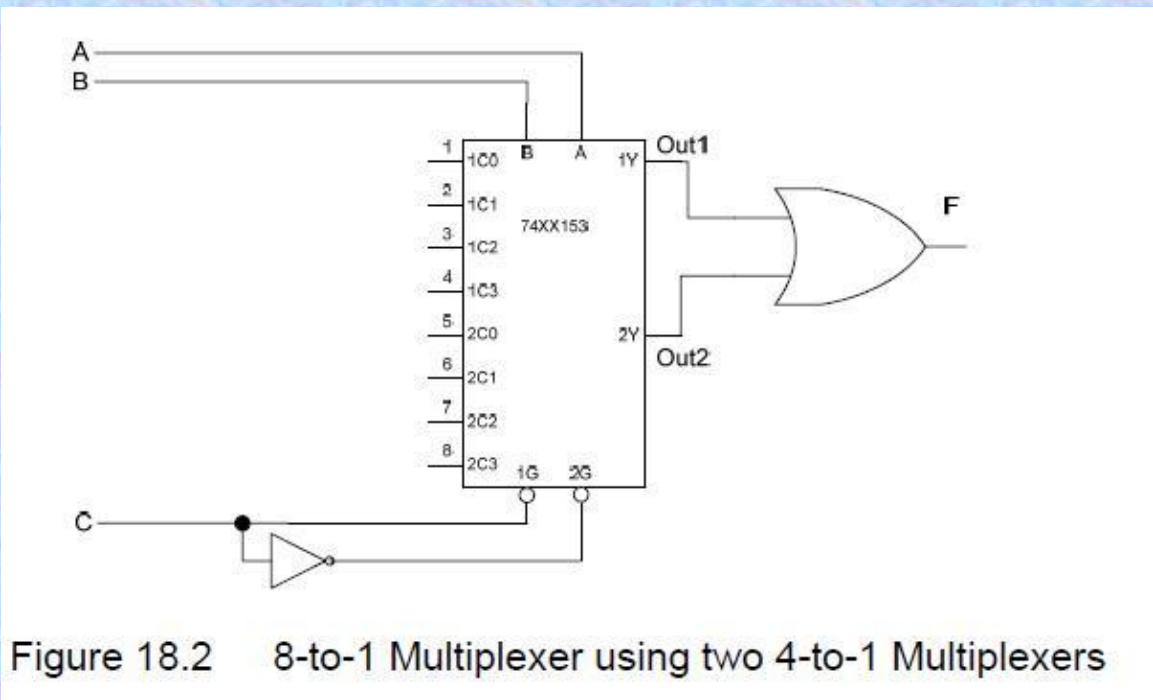


Figure 18.2 8-to-1 Multiplexer using two 4-to-1 Multiplexers

Input			Output
C	B	A	F
0	0	0	1C0
0	0	1	1C1
0	1	0	1C2
0	1	1	1C3
1	0	0	2C0
1	0	1	2C1
1	1	0	2C2
1	1	1	2C3

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

MIDTERM EXAMINATION 2011 (October-November)

Q-21

What is meant by ABEL? (2 marks)

Answer: (Page 201) Lec20

ABEL which is an acronym for Advanced Boolean Expression Language is hardware description language used for implementing logic designs using PLDs.

Q-22

Why preferable to use another method than 5-variable K-Map? (2 marks)

Answer: (Page 102) Lec11

Karnuagh map method becomes difficult to manage when numbers of variables exceed 4. In both the Karnaugh maps, finding the redundant terms is not very obvious. The Quine-McCluskey approach of simplifying Boolean expression is based on an exhaustive search where each minterm is compared with every other minterm in order to remove single variables.

Q-24

Draw circuit diagram of 2-input of 8-bit multiplexer? (3 marks)

Answer: (Page 172) Lec18

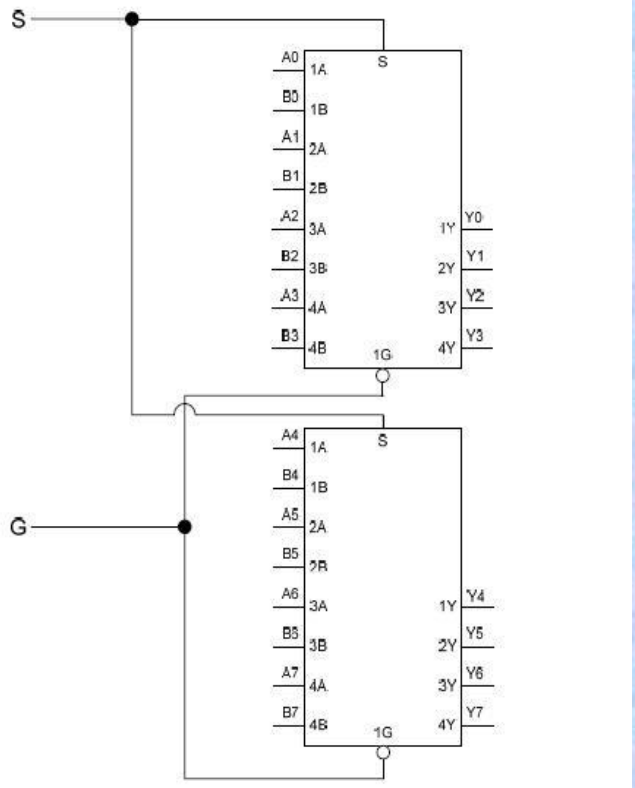


Figure 18.4 2-Input, 8-bit Multiplexer

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Q-25

Uses of Demultiplexer? (5 marks)

Answer: (Page 178) Lec19

Demultiplexer is used to connect a single source to multiple destinations. One use of the Demultiplexer is at the output of the ALU circuit. The output of the ALU has to be stored in one of the multiple registers or storage units. The Data input of the Demultiplexer is connected to the output of the ALU. Each output of the Demultiplexer is connected to each of the multiple registers. By selecting the appropriate output data from the ALU is routed to the appropriate register for storage.

The second use of the Demultiplexer is the reconstruction of Parallel Data from the incoming serial data stream. Serial data arrives at the Data input of the Demultiplexer at fixed time intervals. A counter attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored. When all the bits have been stored, data can be read out in parallel.

MIDTERM EXAMINATION 2011 (October-November)

Q-21

Define Sequential Circuit. MARKS: 2

Answer: (Page 8) Lec1

Digital circuits that generate a new output on the basis of some previously stored information and the new input are known as Sequential circuits.

Digital circuits that use memory elements for their operation are known as Sequential circuits. **(Page 218)**

Q-22

How a circuit with multiple outputs is shown in truth table? MARKS: 2

Answer: (Page 103) Lec11

Circuits having multiple outputs are represented by multiple function tables one for each output or a single function table having multiple output columns. The example of a BCD to 7-Segment Decoder circuit which has 4 inputs and 7 outputs is considered to explain functions having multiple outputs.

Q-23

How decoder is used as demultiplexer. MARKS: 3:

Answer: (Page 178) Lec19

A Demultiplexer is available as a Decoder/Demultiplexer chip which can be configured to operate as a Demultiplexer or a Decoder.

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

MIDTERM EXAMINATION 2011 (October-November)

Q-21

Draw the Tri_state buffer. 2

Answer: (Page 196) Lec20

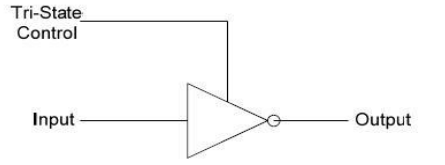
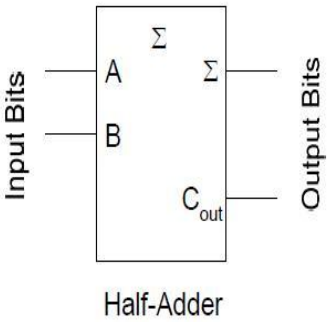


Figure 20.9a Tri-State Buffer

Q-22

Draw the half adder graph. 2

Answer: (Page 134) Lec14



Half-Adder

Q-23

Draw NOR gate based S_R (set rest) Latch. 3

Answer: (Page 220) Lec22

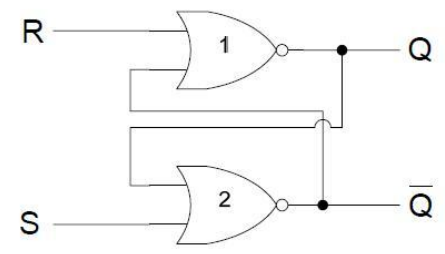


Figure 22.4 NOR based S-R Latch

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

MIDTERM EXAMINATION 2011 (October-November)

Q-22

Two bit comparator? Explain by at least one example

Answer: (Page 109) Lec12

A 2-bit Comparator circuit compares two 2-bit numbers A and B. The comparator circuit has three outputs. It sets the A>B output to 1 if A>B. It sets the A=B output to 1 if A=B and sets A<B output to 1 if A < B.

Q-23

Explain PLDs

Answer: (Page 179) Lec19

Programmable Logic Devices are used in many applications to replace the Logic gates and MSI chips. PLDs save circuit space and reduce and save the cost of components in a Digital Circuit. PLDS consists of Arrays of AND gates and OR gates that can be programmed to perform specific functions.

Q-24

Comparator All possibilities for A = B.

Answer: (Page 109) Lec12

• The output A=B is set to 1 when the input combinations are 00 00, 01 01, 10 10 and 11 11

Q-25

one diagram for PLD array with its fuses connecting columns to rows

Answer: (Page 180) Lec19

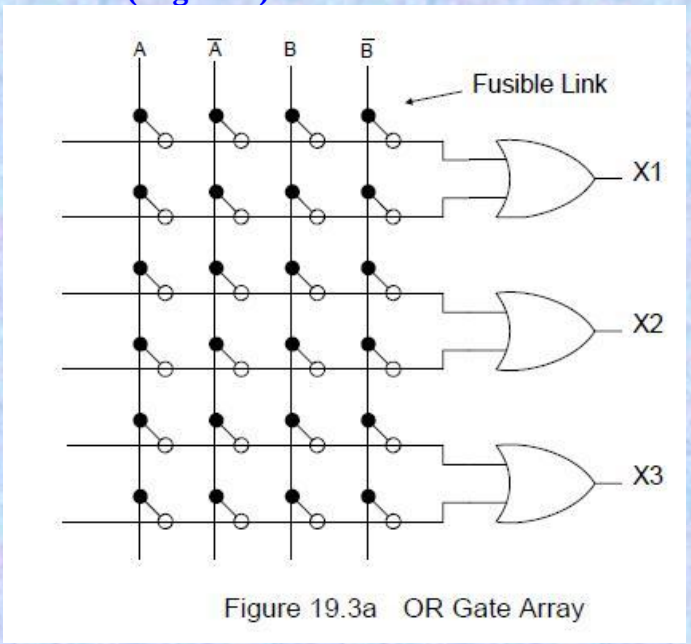


Figure 19.3a OR Gate Array

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

MIDTERM EXAMINATION 2011(May)

Define decoder 2 marks

Answer:- (Page 157)

A Decoder has multiple inputs and multiple outputs. The Decoder device accepts as an input a multi-bit code and activates one or more of its outputs to indicate the presence of the multi-bit code.

Why S and R input of NAND based latch should not be at logic high at same time 2 marks

Answer:- (Page 220)

When inputs are S = 1 and R = 0 the output Q is set to 0. Inputs S = 0 and R = 0 are not applied as they place the latch in an invalid state. The NAND gate based S-R latch has active-low inputs."

2 input 4 bit multiplexer function table 3 marks

Answer:- (Page 169)

Inputs		Outputs			
G	S	1Y	2Y	3Y	4Y
1	X	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

Table 18.1 Function table of 2-Input 4-Bit Multiplexer

Half adder explanation its function table Boolean expression and circuit diagram 5 marks

Answer:- (Page 134)

Half-Adder

A Half-Adder can be fully described in terms of its Function table, its Sum and Carry Out Boolean Expressions and the circuit Implementation.

Half-Adder Function Table

The Half-Adder has a 2-bit input and a 2-bit output. The function table of the Half-Adder has two input columns representing the two single bit numbers A and B. The function table also has two output columns representing the Sum bit and Carry Out bit.

Half-Adder Sum & Carry Out Boolean Expressions

The Sum and Carry Out expressions of the Half-Adder can be determined from the function table. The Half-Adder Sum and Carry Out outputs are defined by the expressions

$$Sum = \overline{A}B + A\overline{B} = A \oplus B$$
$$CarryOut = AB$$

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

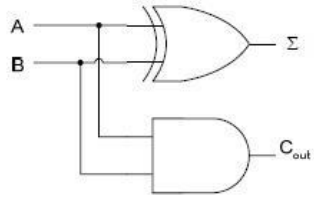


Figure 14.6 Half-Adder Logic Circuit

Explain S-R latch in your own words

Answer:- (Page 218)

A latch is a temporary storage device that has two stable states. A latch output can change from one state to the other by applying appropriate inputs. A latch normally has two inputs, the binary input combinations at the latch input allows the latch to change its state. A latch has two outputs Q and its complement $\overline{Q}$ The latch is said to be in logic high state when Q=1 and $\overline{Q}$ =0 and it is in the logic low state when Q=0 and $\overline{Q}$ =1. When the latch is set to a certain state it retains its state unless the inputs are changed to set the latch to a new state. Thus a latch is a memory element which is able to retain the information stored in it.

MIDTERM EXAMINATION 2011

Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations.

Answer:- (Page 201)

NOT=!
AND= &
OR = #
XOR =$.

MIDTERM EXAMINATION 2010

Question No: 17 (Marks: 2)

Why a 2-bit comparator is called parallel comparator?

Answer:- (Page 154)

The 2-bit Comparator discussed earlier is considered to be a Parallel Comparator as all the bits are compared simultaneously. External Logic has to be used to Cascade together two such Comparators to form a 4-bit Comparator.

Question No: 18 (Marks: 2)

Explain at least two advantages of the circuit having low power consumption

Answer:- (Page 65)

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries.
Secondly, low power consumption means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices.

Question No: 19 (Marks: 2)
Name the four OLMC configurations
Answer:- (Page 196)
The four OLMC configurations are

- Combination Mode with active-low output
- Combinational Mode with active-high output
- Registered Mode with active-low output
- Registered Mode with active-high output

Question No: 20 (Marks: 3)
Explain "Test Vector" in context of ABEL
Answer:- (Page 204)
Once the Logic circuit design has been entered its operation is verified by using 'test vectors'. A 'test vector' specifies the inputs and the corresponding outputs. The software simulates the operation of the logic circuit by applying the test vector and checking the outputs. Test vectors are essentially the same as Truth Tables

Question No: 21 (Marks: 3)
For a two bit comparator circuit specify the inputs for which the output A < B is set to 1
Answer:- (Page 109)
The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

Question No: 22 (Marks: 5)
Explain Tri-State Buffers with the help of block diagram
Answer:- (Page 196)
Tri-State Buffer is a NOT gate with a control line that disconnects the output from the input. When the control line is high the buffer operates like a NOT gate and when the control line is low the output is disconnected from the output and high impedance is seen at the output. Tri-state buffers are used to disconnect the outputs of devices which are connected or share a common output line.

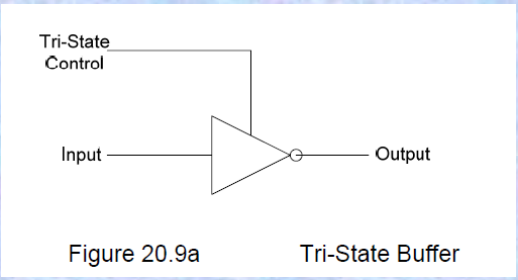


Figure 20.9a Tri-State Buffer

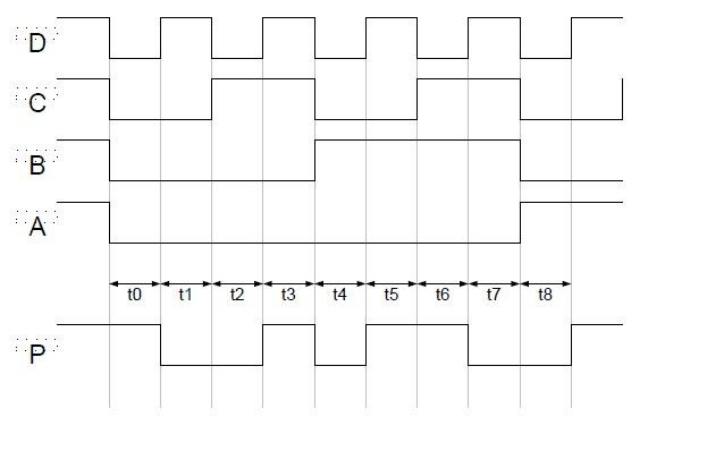
Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 23 (Marks: 5)

Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram

Answer:- (Page 196)

The timing diagram shows the operation of the Odd-Parity generator circuit.
The A, B, C and D timing diagrams represent the changing 4-bit data values. During time interval t0 the 4-bit data value is 0000, during time interval t1, the data value changes to 0001.
Similarly during time intervals t2, t3, t4 up to t8 the data values change to 0010, 0011, 0100 and 1000 respectively. During interval t0 the output of the two XOR gates is 0 and 0, therefore the output of the XNOR gate is 1. At interval t1, the outputs of the two XOR gates is 1 and 0, therefore the output of the XNOR gate is 0. The output P can similarly be traced for intervals t2 to t8.



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Question No: 17 (Marks: 2)

For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination.

$$\overline{A.\overline{B} + \overline{A}.\overline{B}.C.D}$$

Answer:-

The Multiplexers are used to route the contents of any two registers to the ALU inputs. Many Audio signals in telephone network. Computer use Dynamic Memory addressing using same address line for row and column addressing to access data.

Question No: 18 (Marks: 2)

Provide some of the inputs for which the adjacent 1s detector circuit have active high output?

Answer:- (Page 123)

The Adjacent 1s Detector accepts 4-bit inputs.
If two adjacent 1s are detected in the input, the output is set to high.
input combinations will be 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111
The output function is a 1.

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 19 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

Answer:- (Page 222)

Input		Output
S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	invalid

Table 22.3 Truth-Table of NOR based S-R Latch

Question No: 20 (Marks: 3)

For a two bit comparator circuit specify the inputs for which A > B

Answer:- (Page 109)

The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

Question No: 21 (Marks: 3)

Draw the circuit diagram of NOR based S-R Latch ?

Answer:- (Page 220)

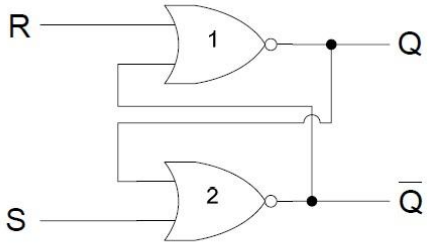


Figure 22.4 NOR based S-R Latch

Question No: 22 (Marks: 5)

One of the ABEL entry methods uses logic equations; explain it with at least a single example.

Answer: (Page 201)

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'. All ABEL equations must end with ';'.

Examples:-

(a) $X = A\bar{B}C + \overline{ABC} + AB + \bar{B}C$

(b) $Y = (\bar{A} + B + \bar{C} + D)(A + B + C)$

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Solution
(a)X = A& !B & C # !A & !B & !C # A & B # !B & C;
(b)Y = (!A # B # !C #D) & (A # B # C);

Question No: 23 (Marks: 5)
Explain Carry propagation in Parallel binary adder?
Answer: (Page 137)
Parallel Binary Adders can be implemented by connecting the required number of 1-bit full adders in a configuration represented in figure 14.9. However, there is a practical limitation to the number of 1-bit Full-Adders that can be connected in parallel. In the 4-bit Parallel Adder, the Most significant bit adder which adds bits A3, B3 and the Carry bit C3, cannot proceed until it receives the Carry from the next least significant 1-bit adder which adds bits A2, B2. The A2, B2 bit adder cannot precede unless it receives the carry input C2 from the A1, B1 adder. The A1, B1 adder in tern depends on A0, B0 adder to provide the carry input. Thus the carry has to propagate through each Full-adder before it reaches the last or most significant full adder.

MIDTERM EXAMINATION 2010

"Write the uses of multiplexer". 2 marks
Answer: (Page 167)
Multiplexer is a digital switch that has several inputs and a single output. Multiplexers are also known as Data Selectors. The main use of the Multiplexer is to select data from multiple sources and to route it to a single Destination

"Write any two advantages of Boolean expressions". 2 marks
Answer: (Page 71)
Boolean expressions which represent Boolean functions help in two ways. The function and operation of a Logic Circuit can be determined by Boolean expressions without implementing the Logic Circuit. Secondly, Logic circuits can be very large and complex. Such large circuits having many gates can be simplified and implemented using fewer gates.

"Draw the diagram of odd parity generator circuit". 2 marks
Answer: (Page 132)

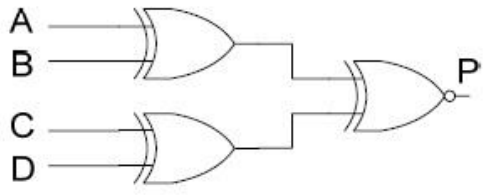


Figure 14.2 Odd-Parity Generator Circuit

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

"What does a 8-bit adder/subtracter circuit do"? 3 marks

Answer: (Page 146)

The Add/Subtract function select input are tied together. The Carry In of the 1st 4-bit Adder circuit is connected to the Add/Subtract function select input. The Carry Out of the 1st 4-bit Adder circuit is connected to the Carry In of the 2nd 4-bit Adder circuit.

"Draw the function table of 3 to 8 decoder". 3 marks

Answer: (Page 160)

Inputs						Outputs							
G1	G2A	G2B	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

"Describe 16 bit ALU". 5 marks

Answer: (Page 151)

The inputs A, B and the output F of the four, 4-bit ALUs 0, 1, 2 and 3 are connected to appropriate bits of the 16-bit inputs A, B and output F respectively. Thus bits A(0-3), B(0-3)and F(0-3) are connected to inputs and output of ALU0, bits A(4-7), B(4-7) and F(4-7) are connected to inputs and output of ALU1, bits A(8-11), B(8-11) and F(8-11) are connected to inputs and output of ALU2 and bits A(12-15), B(12-15) and F(12-15) are connected to inputs and output of ALU3. The Group-Carry Generate and Propagate outputs of the four ALUs are connected to the inputs of Look-Ahead Carry generator 74X182 respectively. The Carry outputs C1, C2 and C3 from the Look-Ahead Carry generator circuit are generated after a gate delay of 2 and are connected to the Carry in pins of ALUS 1, 2 and 3 respectively.

"Describe in your own words about latches". 5 marks

Answer: (repeated)

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Question No: 17 (Marks: 1)

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Briefly state the basic principle of Repeated Division-by-2 method.
Answer: (Page 17)
Repeated Division-by-2 method allows decimal numbers of any magnitude to be converted into binary.

Question No: 18 (Marks: 1)
Briefly state the basic principle of Repeated Multiplication-by-2 Method.
Answer: Page 17
Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.

Question No: 19 (Marks: 2)
Draw the circuit diagram of a Tri-State buffer.
Answer: (Repeated)

Question No: 20 (Marks: 3)
Add -13 and +7 by converting them in binary system your result must be in binary.

Question No: 21 (Marks: 5)
Explain "Sum of Weights" method with example for "Octal to Decimal" conversion
Answer: (Page 14) (Page 33)
In the Sum-of-Weights method an extended expression is written in terms of the Binary Base Number 2 and the weights of the Binary number to be converted. The weights correspond to each of the binary bits which are multiplied by the corresponding binary value.Binary bits having the value 0 do not contribute any value towards the final sum expression.

An Octal number can be directly converted into Decimal by using the sum of weights method. The conversion steps using the Sum-of-Weights method are shown.

4033	Octal number
$4 \times 8_3 + 0 \times 8_2 + 3 \times 8_1 + 3 \times 8_0$	Writing the number in an expression
$(4 \times 512) + (0 \times 64) + (3 \times 8) + (3 \times 1)$	
$2048 + 0 + 24 + 3$	Summing the Weights
2075	Decimal equivalent

Question No: 22 (Marks: 10)
Explain the Implementation of an Odd-Parity Generator Circuit i.e by drawing function table, maping it to K-map and then simplifying the expression.

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Question No: 17 (Marks: 1)

Briefly state the basic principle of Repeated Multiplication-by-2 Method.
Answer: (Repeated)

Question No: 18 (Marks: 1)

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

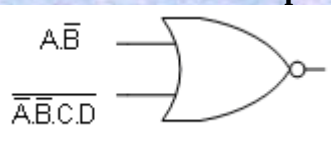
How standard Boolean expressions can be converted into truth table format.

Answer: (Page 87)

All standard Boolean expressions can be easily converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Question No: 19 (Marks: 2)

What will be the out put of the diagram given below



Question No: 20 (Marks: 3)

When an Input (source) file is created in ABEL a module is created which has three sections. Name These three sections.

Answer: (Page 205)

1. Declarations
2. Logic Descriptions
3. Test Vectors

Question No: 21 (Marks: 5)

Explain "AND" Gate and some of its uses

Answer: (Page 40)

The AND Gate performs a logical multiplication function. An AND Gate has multiple inputs and a single output. Most commonly used AND Gates are two input AND gates.

An important use of an AND gate in addition to the multiplication operation is its use to disable or enable a device. Counter device counts from 0 to 100. The counter device increments its current count value to the next when it receives a pulse at its clock input.

Question No: 22 (Marks: 10)

Write down different situations where we need the sequential circuits.

Answer: (Page 217)

This type of system uses storage elements called flip-flops that are employed to change their binary value only at discrete instants of time. Synchronous sequential circuits use logic gates and flip-flop storage devices. Sequential circuits have a clock signal as one of their inputs. All state transitions in such circuits occur only when the clock value is either 0 or 1 or happen at the rising or falling edges of the clock depending on the type of memory elements used in the circuit.

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Question No: 17 (Marks: 1)

How can a PLD be programmed?

Answer: (Page 194)

PLDs are programmed with the help of computer which runs the programming software. The computer is

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

Question No: 18 (Marks: 1)
How many input and output bits do a Half-Adder contain?
Answer: (Page 134):
The Half-Adder has a 2 input bits and 2 output bits.

Question No: 19 (Marks: 2)
Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?
Answer: (Page 178)
The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit.

Question No: 20 (Marks: 3)
Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.
Answer: (repeated)

Question No: 21 (Marks: 5)
Explain with example how noise affects Operation of a CMOS AND Gate circuit.
Answer: (Page 123)
Two CMOS 5 volt series AND gates are connected together. Figure 7.3 The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid VOH range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

Question No: 22 (Marks: 10)
Explain the SOP based implementation of the Adjacent 1s Detector Circuit
Answer: (Page 123)

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in the input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111 the output function is a 1.

Implementing the circuit directly from the function table based on the SOP form requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3. The total gate count is

- One 8 input OR gate
- Eight 4 input AND gates
- Ten NOT gates

The expression can be simplified using a Karnaugh map, figure 13.4, and then the simplified expression can be implemented to reduce the gate count. The simplified expression is$AB + CD + BC$. The circuit implemented using the expression $AB + CD + BC$ has reduced to 3 input OR gate and 2 input AND gates. Figure 13.5

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

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Question No: 17 (Marks: 1)
Which device performs an operation which is the opposite of the Decoder function?
Answer: (Page 163)
An Encoder functional device performs an operation which is the opposite of the Decoder function.

Question No: 18 (Marks: 1)
Name any two modes in which PALs are programmed.
Answer: (Page 199)
The three modes in which PALs are programmed are
• Simple
• Complex
• Registered

Question No: 19 (Marks: 2)
Explain Combinational Function Devices?
Answer: (Page 133)
Digital circuits are formed by the combination of Logic Gates. Xor, Xnor, NAND, NOR are combinational function devices.

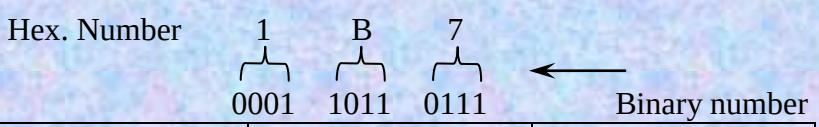
Question No: 20 (Marks: 3)
Differentiate between hexadecimal and octal number system
Answer:
Octa decimal use Base 8 whereas Hexa decimal use Base 16

Question No: 21 (Marks: 5)
Explain "Sum-of-Weights Method" for Hexadecimal to Decimal Conversion with at least one example?
Answer:
The hexadecimal (Hex) numbering system provides even shorter notation than octal. Hexadecimal uses a base of 16. It employs 16 digits: number 0 through 9, and letters A through F, with A through F substituted for numbers 10 to 15, respectively,
Hexadecimal numbers can be expressed as their decimal equivalents by using the sum of weights method, as shown in the following example:

Weight	2	1	0	
Hex. Number	1	B	7	
				$7 \times 16^0 = 7 \times 1 = 7$
				$11 \times 16^1 = 11 \times 16 = 176$
				$1 \times 16^2 = 1 \times 256 = 256$
		Sum of products		439_{10}

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Like octal numbers, hexadecimal numbers can easily be converted to binary or vise versa. Conversion is accomplished by writing the 4-bit binary equivalent of the hex digit for each position, as illustrated in the following example:



Hexadecimal	Binary	Decimal
0	0000	0
1	**0001**	**1**
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	**0111**	**7**
8	1000	8
9	1001	9
A	1010	10
B	**1011**	**11**
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Question No: 22 (Marks: 10)

Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression for (A > B)

Answer: (Page 109)

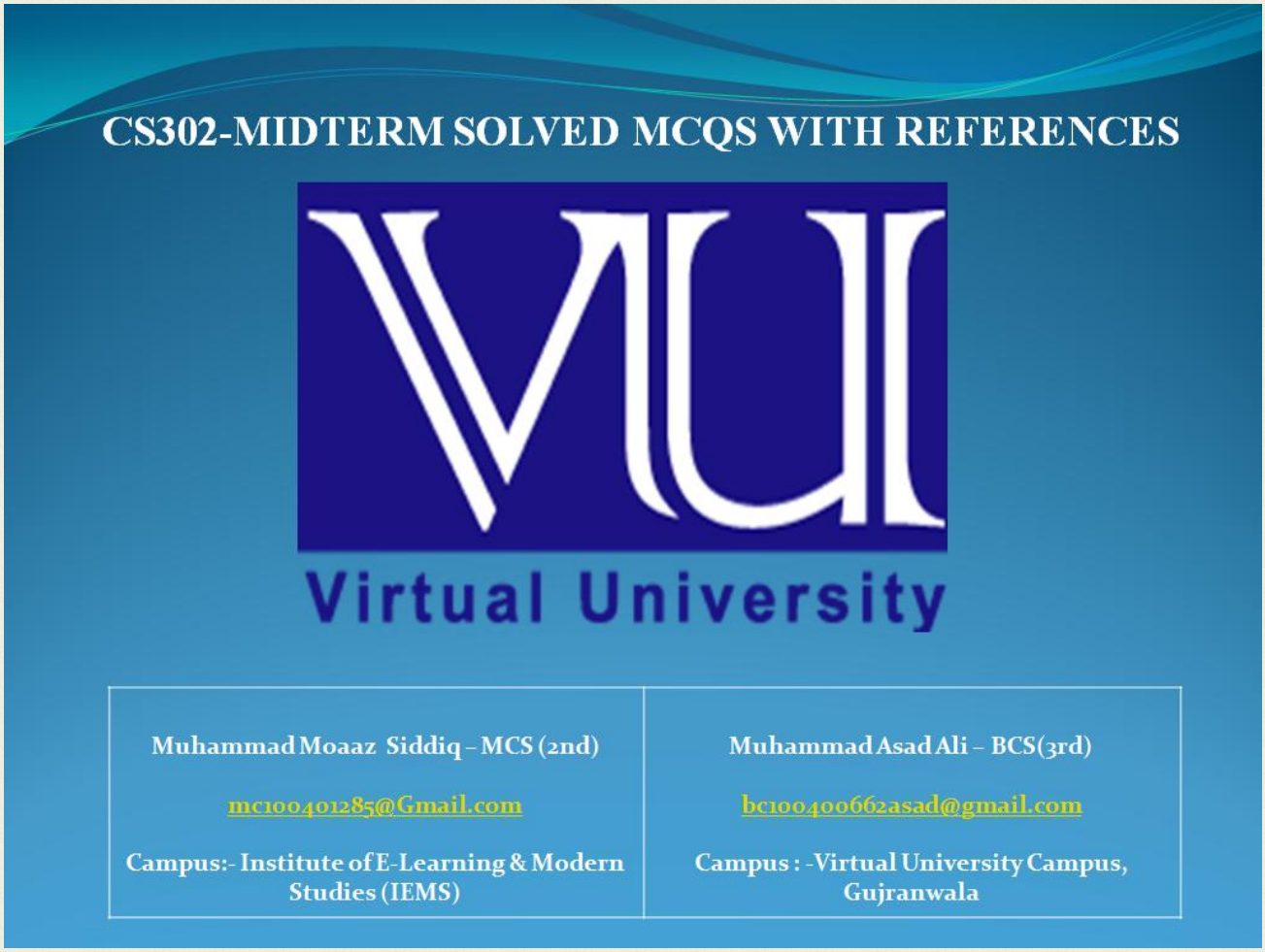
Input				Output		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

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MIDTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► When one or more product terms in the expression are equal to 1. (Page 86)

Question No: 2 (Marks: 1) - Please choose one
The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10 (Page 109)

Question No: 3 (Marks: 1) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► True (Page 154)
► False

Question No: 4 (Marks: 1) - Please choose one
High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► 0.9 V (Page 65)
► 3.3 V

Question No: 5 (Marks: 1) - Please choose one
If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582 (But not sure)
► 2.4582
► 24582

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS)

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

► 0.24582

Question No: 6 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined
► One
► Zero
► 10 (binary)

Question No: 7 (Marks: 1) - Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET (page 220)
► RESET
► Clear
► Invalid

Question No: 8 (Marks: 1) - Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► Fast switching speeds, very low power dissipation (page61)
► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

► 86 (According to Formula)
► 87
► 88
► 89

Question No: 10 (Marks: 1) - Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal

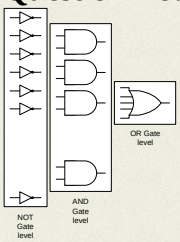
► **Decimal-to-BCD Priority (Page 166)**

Question No: 11 (Marks: 1) - Please choose one

How many data select lines are required for selecting eight inputs?

► 1
► 2
► **3 click here for detail**
► 4

Question No: 12 (Marks: 1) - Please choose one



the diagram above shows the general implementation of _____ form

► boolean
► arbitrary
► POS
► **SOP**

Question No: 13 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

► **4 (Page 217)**
► 8
► 12
► 16

Question No: 14 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs. (Page 178)**
► Multiple inputs and single output.

Question No: 15 (Marks: 1) - Please choose one

The expression _____ is an example of Commutative Law for Multiplication.

► AB+C = A+BC
► A(B+C) = B(A+C)
► **AB=BA (Page 72)**
► A+B=B+A

Question No: 16 (Marks: 1) - Please choose one
"Sum-of-Weights" method is used _____
► **to convert from one number system to other (Page 14)**
► to encode data
► to decode data
► to convert from serial to parralel data

MIDTERM EXAMINATION
Spring 2010

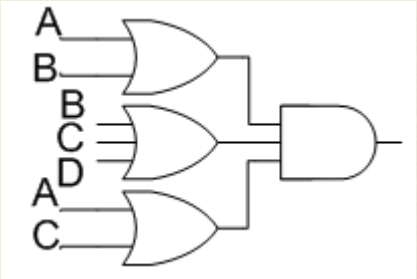
Question No: 1 (Marks: 1) - Please choose one
The maximum number that can be represented using unsigned octal system is _____

► 1
► **7 (Page 31)**
► 9
► 16

Question No: 2 (Marks: 1) - Please choose one
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► **2 (Page 26)**
► 3

Question No: 3 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law

► Associative law
► **Product of sum form (According to rule of theorem)**
► Sum of product form

Question No: 4 (Marks: 1) - Please choose one
The range of Excess-8 code is from _____ to _____
► **+7 to -8 (Page 34)**
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____
► $A+\overline{A}=1$
► $A\overline{A} = 0$ **(Page 85)**
► $1+A=1$
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
► 4
► **8 (Page 89)**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
► **A > B = 1, A < B = 0, A < B = 1**
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one
A particular Full Adder has
► **3 inputs and 2 output (Page 135)**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as _____

► **Function Select Inputs (Page 147)**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement (Page 144)**

► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR (Page 186)**

MIDTERM EXAMINATION 2010

1. **The binary value "11011" is equivalent to _____**

►**1B (According to rule)**
►1C
►1D
►1E

2. **An important application of AND Gate is its use in counter circuit**

►**True (Page 281)**
►False

3. **The OR Gate performs a Boolean _____ function**

►**Addition (Page 42)**
►Subtraction
►Multiplication
►Division

4. **TTL based devices work with a dc supply of ____ Volts**

►+10
►**+5 (Page 61)**
►+3

Muhammad Moaaz Siddiq – MCS (2nd)	Muhammad Asad Ali – BCS(3rd)
mc100401285@Gmail.com	bc100400662asad@gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS)	Campus : -Virtual University Campus, Gujranwala

►3.3

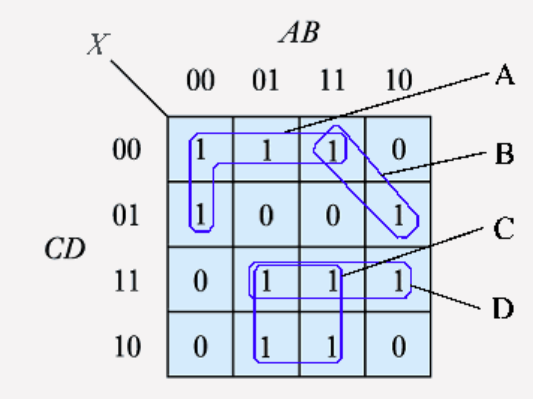
5. A standard POS form has _____ terms that have all the variables in the domain of the expression.

►**Sum (Page 85)**
►Product
►Min
►Composite

6. A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.

►2
►4
►**8 (According to rule)**
►16

7. A BCD to 7-Segment decoder has
►3 inputs and 7 outputs
►**4 inputs and 7 outputs (Page 103)**
►7 inputs and 3 outputs
► inputs and 4 outputs



8. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?

►A
►
►**C click here for detail**
►D

9. The binary value of 1010 is converted to the product term $\bar{A}B\bar{C}D$

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS)

Muhammad Asad Ali – BCS(3rd)
bc100400662asad@gmail.com
Campus : -Virtual University Campus, Gujranwala

►True
►**False**

10. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

►A > B = 1, A < B = 0, A < B = 1
►A > B = 0, A < B = 1, A = B = 0
►**A > B = 1, A < B = 0, A = B = 0 (Page 109)**
►A > B = 0, A < B = 1, A = B = 1

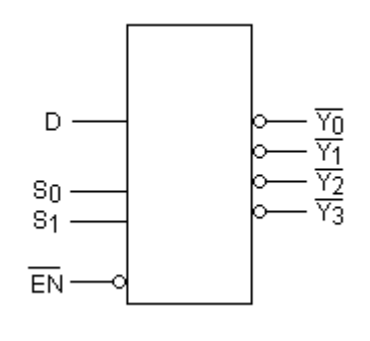
11. $C_{out1} + S_3(S_2 + S_1)$ **is boolean expression for**

►Half Adder
►Full Adder
►**The Invalid BCD Detector Circuit (page 142)**
►Parity Checker

12. 3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

►**True (Page 160)**
►False

13. The device shown here is most likely a _____



►Comparator
►Multiplexer
►**Demultiplexer click here for detail**
►Parity generator

14. The GAL22V10 has ____ inputs

►**22 (Page 195)**
►10
►44
►20

15. A latch retains the state unless

►Power is turned off
►**Input is changed (page 218)**
►Output is changed
►Clock pulse is changed

16. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

►**SET (Page 220)**
►RESET
►Clear
►Invalid

17. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (V_{oH}) will be in the range of _____ volts.

►4 to 4.5
►**4.5 to 5**
►0 to 4.5
►0 to 3.5

18. A.(B.C) = (A.B).C is an expression of _____

►Demorgan's Law
►Distributive Law
►Commutative Law
►**Associative Law (Page 72)**

19. The 4-bit 2's complement representation of "+5" is _____

►1010
►1110
►**1011**
►0101

20. Which of the number is not a representative of hexadecimal system

►1234
►ABCD
►1001
►DEHF Hexa does not have H as remainder

MIDTERM EXAMINATION
Spring 2010

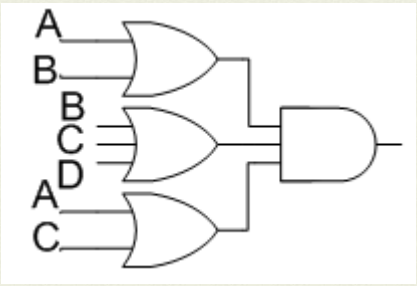
Question No: 1 (Marks: 1) - Please choose one

► 1
► **7**
► 9
► 16

Question No: 2 (Marks: 1) - Please choose one
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► 2 (Page 26)
► 3

Question No: 3 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form (According to rule)
► Sum of product form

Question No: 4 (Marks: 1) - Please choose one

The range of Excess-8 code is from _____ to _____

► **+7 to -8 (Page 34)**
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____

► $A+\overline{A}=1$
► $A\overline{A}=0$ **(Page 85)**
► $1+A=1$
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8 (Page 89)**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one
A particular Full Adder has

► **3 inputs and 2 output (Page 135)**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as ____

► **Function Select Inputs (Page 147)**

► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► **16**

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement (Page 144)**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one

The binary value “1010110” is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

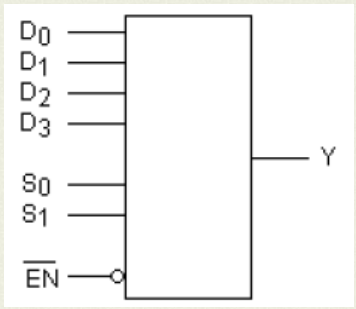
► AND
► OR
► **NOT (page 196)**
► **XOR**

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

Question No: 1 (Marks: 1) - Please choose one
GALcan be reprogrammed because instead of fuses _____logic is used in it

► **E^2CMOS (Page 191)**
► TTL
► CMOS+
► **None of the given options**

Question No: 2 (Marks: 1) - Please choose one
The device shown here is most likely a



► Comparator
► **Multiplexer** **click here for detail**
► Demultiplexer
► Parity generator

Question No: 3 (Marks: 1) - Please choose one
If“1110” is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2^{nd}
► 4^{th}

► 14^{th}

► **No output wire will be activated (Page 163)**

Question No: 4 (Marks: 1) - Please choose one

Half-Adder Logic circuit contains 2 XOR Gates

► True

► **False (Page 135)**

Question No: 5 (Marks: 1) - Please choose one

A particular Full Adder has

► **3 inputs and 2 output (Page 135)**

► 3 inputs and 3 output

► 2 inputs and 3 output

► **2 inputs and 2 output**

Question No: 6 (Marks: 1) - Please choose one

$Sum = A \oplus B \oplus C$

$CarryOut = C(A \oplus B) + AB$

are the Sum and CarryOut expression of

► Half Adder

► **Full Adder (Page 135)**

► 3-bit parralel adder

► MSI adder cicuit

Question No: 7 (Marks: 1) - Please choose one

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True** click here for detail

► **False**

Question No: 8 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01

► A=11, B=01

► A=01, B=01

► **A=01, B=10 (Page 109)**

Question No: 9 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____cells for min or max terms

► 4

► 8

► 12

► 16 (Page 90)

Question No: 10 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____devices remains constant throughout their operation.

► TTL (Page 65)
► CMOS 3.5 series
► CMOS 5 Series
► **Power dissipation of all circuits increases with time.**

Question No: 11 (Marks: 1) - Please choose one
The ecimal "8" is represented as _____using Gray-Code.

► 0011
► 1100 (page 36)
► 1000
► 1010

Question No: 12 (Marks: 1) - Please choose one

(A+B).(A+C) = _____
► B+C
► A+BC (According to rule)
► AB+C
► AC+B

Question No: 13 (Marks: 1) - Please choose one
A.(B+ C) = A.B + A.C is the expression of _____

► Demorgan's Law
► Commutative Law
► Distributive Law (Page 73)
► Associative Law

Question No: 14 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► TRUE (Page 50)

Question No: 15 (Marks: 1) - Please choose one
In ANSI/IEEE Standard 754 "Mantissa" is represented by _____32-bits_____bits

► 8-bits
► 16-bits
► 32-bits (Page 24)

► 64-bits

Question No: 16 (Marks: 1) - Please choose one
Caveman number system is Base _5_____number system

► 2
► 5 (Page 11)
► 10
► 16

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
According to Demorgan's theorem:
$\overline{A + B + C}$ = _____

► A.B.C
► $A + \overline{B.C}$
► $\overline{A}.\overline{B}.\overline{C}$ (Page 74)
► $\overline{A.B} + C$

Question No: 2 (Marks: 1) - Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► 8-bit (Page 38)
► 16-bit

Question No: 3 (Marks: 1) - Please choose one
The AND Gate performs a logical _____function

► Addition
► Subtraction
► Multiplication (Page 40)
► Division

Question No: 4 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____

► OR Gate and then NOT Gate (Page 47)
► NOT Gate and then OR Gate
► AND Gate and then OR Gate

► OR Gate and then AND Gate

Question No: 5 (Marks: 1) - Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL (Page 65)**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 6 (Marks: 1) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True (Page 154)**
► False

Question No: 7 (Marks: 1) - Please choose one
When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► **NOT (Page196)**
► XOR

Question No: 8 (Marks: 1) - Please choose one
The GAL22V10 has ____ inputs

► **22 (Page 195)**
► 10
► 44
► 20

Question No: 9 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is

► !
► &
► **# (Page 201)**
► $

Question No: 10 (Marks: 1) - Please choose one
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements (Page 207)**
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) - Please choose one
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon) (Page 201)**
► " endl " (keyword "endl")

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216) rep**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
"Sum-of-Weights" method is used _____
► **to convert from one number system to other (Page 14)**
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14 (Marks: 1) - Please choose one
Circuits having a bubble at their outputs are considered to have an active-low output.

► **True (Page 128)**
► False

Question No: 15 (Marks: 1) - Please choose one
$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of _____

► **Product of sum form (According to rule)**
► Sum of product form
► Demorgans law
► Associative law

Question No: 16 (Marks: 1) - Please choose one
Which one is true:

► **Power consumption of TTL is higher than of CMOS (Page 61)**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

MIDTERM EXAMINATION
Spring 2009

Question No: 1 (Marks: 1) - Please choose one
In the binary number "10011" the weight of the most significant digit is ____

► **2^4 (2 raise to power 4) (Page 13)**
► 2^3 (2 raise to power 3)
► 2^0 (2 raise to power 0)
► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) - Please choose one
An S-R latch can be implemented by using _____ gates

► AND, OR
► **NAND, NOR (Page 218-220)**
► NAND, XOR
► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one
A latch has _____ stable states

► One
► **Two (Page 218)**
► Three
► Four

Question No: 4 (Marks: 1) - Please choose one
Sequential circuits have storage elements

► **True (Page 8)**
► False

Question No: 5 (Marks: 1) - Please choose one
The ABEL symbol for "XOR" operation is

► **$ (Page 210)**
► #
► !

► &

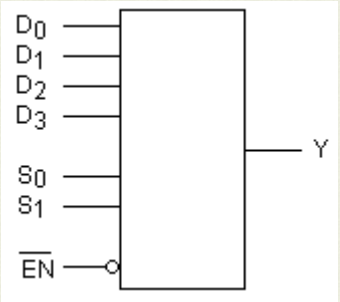
Question No: 6 (Marks: 1) - Please choose one
A Demultiplexer is not available commercially.

► **True (Page 178)**
► False

Question No: 7 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► **A parallel to serial converter circuit (Page 244)**
► A counter circuit
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

Question No: 8 (Marks: 1) - Please choose one
The device shown here is most likely a



► Comparator
► **Multiplexer click here for detail**
► Demultiplexer
► Parity generator

Question No: 9 (Marks: 1) - Please choose one
The main use of the Multiplexer is to

► **Select data from multiple sources and to route it to a single Destination (Page 167)**
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}\,B\,C + A\,\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► two AND gates, one OR gate, two inverters
► two AND gates, one OR gate

Question No: 11 (Marks: 1) - Please choose one
The binary value of 1010 is converted to the product term $\overline{A}B\overline{C}D$

► True
► False

Question No: 12 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8 (Page 89)
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
Following is standard POS expression
$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$

► True (According to logic)
► False

Question No: 14 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

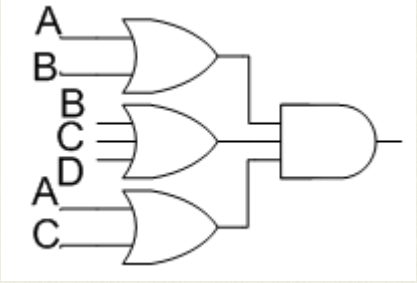
► Undefined
► One
► Zero
► 10 (binary)

Question No: 15 (Marks: 1) - Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit

► **8-bit (Page 38)**
► 16-bit

Question No: 16 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form (According to rule)**
► Sum of product form

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
Which of the number is not a representative of hexadecimal system

► 1234
► ABCD
► 1001
► **DEFH Hexa does not have H as remainder**

Question No: 2 (Marks: 1) - Please choose one
The Unsigned Binary representation can only represent positive binary numbers

► **True (Page 21)**
► False

Question No: 3 (Marks: 1) - Please choose one
The values that exceed the specified range can not be correctly represented and are considered as _____

► **Overflow (Page 23)**
► Carry
► Parity
► Sign value

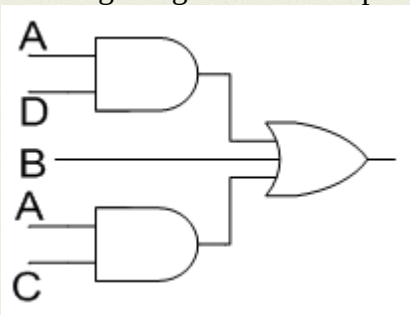
Question No: 4 (Marks: 1) - Please choose one
The 4-bit 2's complement representation of "-7" is _____

► 0111
► 1111
► **1001 (Page 21)**
► 0110

Question No: 5 (Marks: 1) - Please choose one
$\overline{A}B + \overline{A}B\overline{C} + AC$ is an example of _____

► Product of sum form
► **Sum of product form (Page 77)**
► Demorgans law
► Associative law

Question No: 6 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form**

Question No: 7 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 8 (Marks: 1) - Please choose one
The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► **16 (Page 90)**

Question No: 9 (Marks: 1) - Please choose one
A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► **4 inputs and 7 outputs (Page 103)**
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

Question No: 10 (Marks: 1) - Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► **2-input, 4-bit (Page 169)**

Question No: 11 (Marks: 1) - Please choose one
The PROM
consists of a fixed non-programmable _____ Gate array configured as a decoder.

► **AND (Page 182)**
► OR
► NOT
► XOR

Question No: 12 (Marks: 1) - Please choose one
In ABEL the variable 'A' is treated separately from variable 'a'

►

► **True (Page 201)**

► False

Question No: 13 (Marks: 1) - Please choose one

The ABEL notation equivalent to Boolean expression A+B is:

► A & B

► A ! B

► **A # B (Page 201)**

► A $ B

L-21

Question No: 14 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► **SET (Page 220)**

► RESET

► Clear

► Invalid

Question No: 15 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.

► Multiple inputs and multiple outputs.

► **Single input and multiple outputs. (Page 178)**

► Multiple inputs and single output.

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

► **Power consumption of TTL is higher than of CMOS (Page 61)**

► Power consumption of CMOS is higher than of TTL

► Both TTL and CMOS have same power consumption

► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one

The first Least Significant digit in decimal number system has

position 0 and weight equal to 1

position 1 and weight equal to 0

position 1 and weight equal to 10
position 0 and weight equal to 10

Question No: 2 (Marks: 1) - Please choose one
The decimal equivalent of the binary number "10011" is

19 (According to rule)
99
29
None of given options

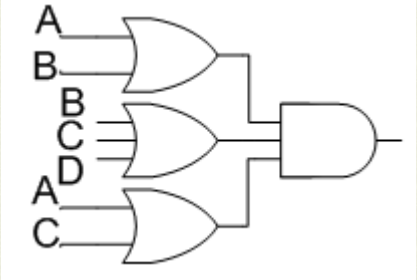
Question No: 3 (Marks: 1) - Please choose one
In ANSI/IEEE Standard 754 "Mantissa" is represented by ____32-bits_____bits

► 8-bits
► 16-bits
► 32-bits (Page 24)
► 64-bits

Question No: 4 (Marks: 1) - Please choose one
The binary value "11011" is equivalent to

1B (According to rule)
1C
1D
1E

Question No: 6 (Marks: 1) - Please choose one
The diagram given below represents



Demorgans law
Associative law
Product of sum form (According to rule)
Sum of product form

Question No: 7 (Marks: 1) - Please choose one
NOR gate is formed by connecting

OR Gate and then NOT Gate (Page 47)
NOT Gate and then OR Gate

AND Gate and then OR Gate
OR Gate and then AND Gate

Question No: 8 (Marks: 1) - Please choose one
"74ALS" stands for

Advanced Low-frequency Schottky TTL
Advanced Low-dissipation Schottky TTL
Advanced Low-Power Schottky TTL (Page 61)
Advanced Low-propagation Schottky TTL

Question No: 9 (Marks: 1) - Please choose one
An adder circuit can be used to perform subtraction operation

True (Page 146)
False

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

2 (Page 160)
3
4
1

Question No: 11 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True Page 161
False

Question No: 12 (Marks: 1) - Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a multiplexer.

2-input, 4-bit
4-input, 8-bit
4-input, 16-bit
2-input, 8-bit (Page 171)

Question No: 13 (Marks: 1) - Please choose one
The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected together through a 4-input gate

AND
OR (Page 171-172)
NAND
XOR

Question No: 14 (Marks: 1) - Please choose one
The Programmable Array Logic (PAL) has AND array and a OR array

Fixed, programmable
Programmable, fixed (Page 182)
Fixed, fixed
Programmable, programmable

Question No: 15 (Marks: 1) - Please choose one
Sequential circuits have storage elements

True (Page 218)
False

Question No: 16 (Marks: 1) - Please choose one
Demultiplexer has

Single input and single outputs.
Multiple inputs and multiple outputs.
Single input and multiple outputs. (Page 178)
Multiple inputs and single output.

For More Visit VUStudents.pk

CS304 Solved Grand Quiz 2020

Question No 1

a'A static member function can be called, when a class is not_____.

Select Correct Option

- ✓ Declared
- ✓ Define
- ✓ **Instantiated**……(For More Visit VUStudents.pk)
- ✓ Called

Question No 2

The _____ relationship indicated that an object contains other objects.

Select Correct Option

- ✓ be
- ✓ is-a
- ✓ has-a
- ✓ **None of the above**……(For More Visit VUStudents.pk)

Question No 3

A generalization relation between classes are implemented using

Select Correct Option

- ✓ Data hiding
- ✓ Friend classes
- ✓ Encapsulation
- ✓ **Inheritance**……(For More Visit VUStudents.pk)

Question No 4

A member function having the same name as that of a class and a ~ sign with it is called,

Select Correct Option

- ✓ Least independencies among modules
- ✓ Implementation independence
- ✓ **Information hiding**……(For More Visit VUStudents.pk)
- ✓ All

For More Visit VUStudents.pk

Question No 5

For classes with common behavior, you can save effort by placing the common behavior in a _____.

Select Correct Option

- ✓ Derived Class
- ✓ **Base Class**……(For More Visit VUStudents.pk)
- ✓ Deprived Class
- ✓ Name Class

Question No 6

Which of the following are an advantage of OOP?

Select Correct Option

- ✓ OOP makes it easy to re-use the code
- ✓ It provides an ability to create one user defined data type by extending the other.
- ✓ It provides the facility of defining Abstract data types through which real world entities can be defined better
- ✓ **All of the above**……(For More Visit VUStudents.pk)

Question No 7

A static member function cannot be declared

Select Correct Option

- ✓ Static
- ✓ Implicit
- ✓ Explicit
- ✓ **Virtual**……(For More Visit VUStudents.pk)

Question No 8

A C++ class is similar to:

Select Correct Option

- ✓ Library File
- ✓ **Structure**……(For More Visit VUStudents.pk)
- ✓ Header File
- ✓ None

Question No 9

Suppose that the Test class does not have an overloaded assignment operator. What happens when an assignment a=b; is given for two Test objects a and b?

Select Correct Option

- ✓ The automatic assignment operator is used
- ✓ The copy constructor is used
- ✓ **Compiler error**……(For More Visit VUStudents.pk)
- ✓ Run-time error

Question No 10

Which operator can not be overloaded?

Select Correct Option

- ✓ The relation operator (>=)
- ✓ Assignment operator (=)
- ✓ Script operator ([])
- ✓ **Conditional operator (?:)** ……(For More Visit VUStudents.pk)

Question No 11

We capture the object attributes and behavior in Object Oriented Programming using:

Select Correct Option

- ✓ Class
- ✓ **Function**……(For More Visit VUStudents.pk)
- ✓ Data Members
- ✓ Instances

Question No 12

A template provides a convenient way to make a family of

Select Correct Option

- ✓ Variables and data members
- ✓ **Function and classes**……(For More Visit VUStudents.pk)
- ✓ Classes and exceptions
- ✓ Programs and algorithms

Question No 13

What is true about function templates?

Select Correct Option

- ✓ The compiler generates only one copy of the function template
- ✓ **The compiler generates a copy of function respective to each type of data**
- ✓ The compiler can only generate copy for the int type data
- ✓ None of the given

Question No 14

If there is a pointer p to objects of a base class, and it contains the address of an object class and both classes contain a novvirtual member function. Ding(), then the statement p->ding(); will cause the version of ding() in the _____ class to be executed.

Select Correct Option

- ✓ Derived
- ✓ Base
- ✓ Abstract
- ✓ **Virtual**……(For More Visit VUStudents.pk)

Question No 15

Which is not the advantage of inheritance?

Select Correct Option

- ✓ Providing class growth through natural selection
- ✓ **Facilitating class libraries**……(For More Visit VUStudents.pk)
- ✓ Avoiding the rewriting of code
- ✓ Providing a useful conceptual framework

Question No 16

What problem(s) may occur when we copy objects without using deep copy constructor?

Select Correct Option

- ✓ Dangling pointer
- ✓ Memory Leakage
- ✓ System crash
- ✓ **All of the given**……(For More Visit VUStudents.pk)

Question No 17

To convert from a user-defined class to a basic type, you would most likely use.

Select Correct Option

- ✓ A built-in conversion operator
- ✓ A one-argument constructor
- ✓ **An overloaded = operator**……(For More Visit VUStudents.pk)
- ✓ A conversion operator that's a member of the class

Question No 18

Friend functions are _____ function of a class.

Select Correct Option

- ✓ Object member
- ✓ **Non-member**……(For More Visit VUStudents.pk)
- ✓ Data member
- ✓ None of the given

Question No 19

The statement objA=objB; will cause a compiler error if the objects are of different classes.

Select Correct Option

- ✓ **True**……(For More Visit VUStudents.pk)
- ✓ False

Question No 20

In object oriented programming, a class of objects cans_____ properties from another class of objects.

Select Correct Option

- ✓ Utilize
- ✓ Borrow
- ✓ **Inherit**……(For More Visit VUStudents.pk)
- ✓ Adopt

Question No 21

_____ satisfy the condition of polymorphism.

Select Correct Option

- ✓ Carbon
- ✓ Diamond
- ✓ Coal
- ✓ **All**……(For More Visit VUStudents.pk)

Question No 22

The >= operator can be overloaded.

Select Correct Option

- ✓ **True**……(For More Visit VUStudents.pk)
- ✓ False

Question No 23

Static variable can be initialized more than once.

Select Correct Option

- ✓ **True**……(For More Visit VUStudents.pk)
- ✓ False

Question No 24

In OOP a class is an example of _____.

Select Correct Option

- ✓ Data type
- ✓ Abstract type
- ✓ **User defined data type**……(For More Visit VUStudents.pk)
- ✓ None of All

Question No 25

The members of a class that can be access without creating the object of the class is called.

Select Correct Option

- ✓ Private member
- ✓ Data member
- ✓ **Public Member**……(For More Visit VUStudents.pk)
- ✓ Static

Question No 26

Suppose there is an object of type Person, which of the following can be considered as one of itsattributes.

Select Correct Option

- ✓ Name
- ✓ Age
- ✓ Work()
- ✓ **Both Name & Age**……(For More Visit VUStudents.pk)

Question No 27

What a derived class can add?

Select Correct Option

- ✓ New data members
- ✓ New member functions and New friend functions
- ✓ New constructors and destructor
- ✓ **All of given**……(For More Visit VUStudents.pk)

Question No 28

_____ is/are used to access information hidden within an object?

Select Correct Option

- ✓ Interface
- ✓ Private data members
- ✓ **Private member functions**……(For More Visit VUStudents.pk)
- ✓ Both public and private members

Question No 29

this pointers are not accessible for static member functions.

Select Correct Option

- ✓ **True**……(For More Visit VUStudents.pk)
- ✓ False

Question No 30

Which of the following operators always takes no argument if overloaded?

Select Correct Option

- ✓ /
- ✓ =……(For More Visit VUStudents.pk)
- ✓ +
- ✓ ++

THE END