Question # 1 of 10 (Start time: 10:02:48 PM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

Question # 2 of 10 (Start time: 10:03:58 PM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:

IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>

Question # 3 of 10 (Start time: 10:04:28 PM) Total Marks: 1
What is the working of Processor Status Word (PSW)?
Select correct option:

To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed

Question # 4 of 10 (Start time: 10:05:10 PM) Total Marks: 1
What does the instruction "ldr R3, 58" of SRC do?
Select correct option:

It will load the register R3 with the contents of the memory location M [PC+58]
It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation

Question # 5 of 10 (Start time: 10:06:34 PM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 6 of 10 (Start time: 10:06:57 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

Question # 8 of 10 (Start time: 10:07:36 PM) Total Marks: 1
For the _____ type instructions, we require a register to hold the data that is to be loaded from the

memory, or stored back to the memory
Select correct option:

Jump
Control
load/store
None of the given

Question # 9 of 10 (Start time: 10:08:08 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:

Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 10 of 10 (Start time: 10:08:50 PM) Total Marks: 1
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register **B)** from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Question # 1 of 10 (Start time: 10:20:53 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:

Logic Design Level
Circuit Level
Mask Level
None of the given

Question # 2 of 10 (Start time: 10:21:17 PM) Total Marks: 1
The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
Select correct option:

Jump and branch format instructions
Immediate format instructions
Register format instructions
All of the above

Question # 5 of 10 (Start time: 10:24:08 PM) Total Marks: 1
P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
Select correct option:

Parentheses ()
Arrow <-
Colon :
Comma ,

Question # 6 of 10 (Start time: 10:25:09 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:

Arithmetic/logic
Load/store
Test/branch
None of the given

What does the word 'D' in the 'D-flip-Flop' stands for?
Select correct option:

Data
Digital
Dynamic
Double

Question # 9 of 10 (Start time: 10:27:24 PM) Total Marks: 1
The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
Select correct option:

Add R3, 56
lar R3, 56
ldr R3, 56
str R3, 56

Question # 10 of 10 (Start time: 10:28:07 PM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 2 of 10 (Start time: 10:41:07 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

Question # 3 of 10 (Start time: 10:41:57 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

Question # 4 of 10 (Start time: 10:42:17 PM) Total Marks: 1
Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
Select correct option:

:=
&
%
©

Question # 5 of 10 (Start time: 10:42:37 PM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

Question # 7 of 10 (Start time: 10:43:25 PM) Total Marks: 1
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Select correct option:

compiler
cross assembler
debugger
linker

Question # 8 of 10 (Start time: 10:43:59 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:

ld instruction
ldr instruction
lar instruction
str instruction

Question # 9 of 10 (Start time: 10:44:37 PM) Total Marks: 1
What does the instruction "ldr R3, 58" of SRC do?
Select correct option:

It will load the register R3 with the contents of the memory location M [PC+58]
It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation

Question # 1 of 10 (Start time: 11:06:09 PM) Total Marks: 1
Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?
Select correct option:
Base address
Binary address
Effective address
All of the given

Quiz Start Time: 11:06 PM
Time Left 88
sec(s)
Question # 2 of 10 (Start time: 11:06:53 PM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:
IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>

Question # 3 of 10 (Start time: 11:07:32 PM) Total Marks: 1
What functionality is performed by the instruction "str R8, 34" of SRC?
Select correct option:
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).
It will store the register R8 contents to the memory location M [PC+34]
No operation

Question # 4 of 10 (Start time: 11:08:39 PM) Total Marks: 1
Which type of instructions help in changing the flow of the program as and when required?
Select correct option:
Arithmetic
Control
Data transfer
Floating point

Question # 5 of 10 (Start time: 11:09:24 PM) Total Marks: 1
Whic of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPUs.
Select correct option:
(a), (b) &(c)
(b), (c) & (e)
(c), (d) & (e)
(a), (c) & (d)

Question # 8 of 10 (Start time: 11:11:44 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 9 of 10 (Start time: 11:12:32 PM) Total Marks: 1
Which one of the following is/are the features of Register Transfer Language? a) It is a symbolic language b) It is describing the internal organization of digital computers c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers d) It is high level language
Select correct option:
(b) only
(a) & (b) only

(a) ,(b) & (d)
(b),(c) & (d)

Question # 10 of 10 (Start time: 11:14:04 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

Question # 3 of 10 (Start time: 08:03:34 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:

CISC
RISC
SRC
FALCON

Question # 5 of 10 (Start time: 08:05:09 PM) Total Marks: 1
Which one of the following registers holds the instruction that is being executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 9 of 10 (Start time: 08:08:13 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Question # 10 of 10 (Start time: 08:09:02 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 1 of 10 (Start time: 08:18:13 PM) Total Marks: 1

Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 2 of 10 (Start time: 08:18:29 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:

Perfecting
Pipelining
Superscalar operation
Speedup

Question # 3 of 10 (Start time: 08:18:52 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

vu39

Question # 4 of 10 (Start time: 08:19:03 PM) Total Marks: 1
The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------
Select correct option:

Exception
Function
Thread
Stack

Question # 5 of 10 (Start time: 08:20:13 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 6 of 10 (Start time: 08:20:40 PM) Total Marks: 1

_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 7 of 10 (Start time: 08:21:15 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 8 of 10 (Start time: 08:21:49 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:

Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously

Question # 9 of 10 (Start time: 08:22:09 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ address bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:22:19 PM) Total Marks: 1
Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 1 of 10 (Start time: 08:24:34 PM) Total Marks: 1
---------- performs the data operations as commanded by the program instructions.
Select correct option:

Control

Datapath
Structural RTL
Timing

Question # 2 of 10 (Start time: 08:25:17 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 3 of 10 (Start time: 08:25:30 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:

8-bit , 8-bit
16-bit , 16-bit
16-bit , 24-bit
16-bit , 32-bit

Question # 4 of 10 (Start time: 08:25:50 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 5 of 10 (Start time: 08:26:02 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 6 of 10 (Start time: 08:26:41 PM) Total Marks: 1
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 7 of 10 (Start time: 08:27:38 PM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:

vu39

8-bits
16-bits
32-bits
64-bits

Question # 8 of 10 (Start time: 08:27:54 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

Question # 9 of 10 (Start time: 08:28:10 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:28:29 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

vu39