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CS302 QUIZ 1 SOLVED

Provide by VU Answer

1. The terminal count of a 4-bit binary counter in the UP mode is___.

a) 1100

b) 0011

c) 1111

d) 0000

2. For a down counter that counts from (111 to 000). If current state is “101” the next state willbe__.

a) 111

b) 110

c) 010

d) None of given options

3. The n flip-flops store___states.

a) 1

b) 2^n

c) 0

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d) 2^(n+1)

4. An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting _____.

a) Q output of all flip-flops to clock input of next flip-flops

b) Q' output of all flip-flops to clock input of next flip-flops

c) Q output of all flip-flops to J input of next flip-flops

d) Q' output of all flip-flops to K input of next flip-flops

5. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the IntegratedCircuit counters allow cascading of multiple counters together.

a) True

b) False

6. A decade counter can be implemented by truncating the counting sequence of a MOD-20counter.

a) True

b) False

7. The 74HC163 is a 4-bit Synchronous Counter, it has_____data output pins.

a) 2

b) 4

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c) 6

d) 8

8. _____Counters as the name indicates are not triggered simultaneously

a) Asynchronous

b) Synchronous

c) Positive-Edge triggered

d) Negative-Edge triggered

9. Divide-by-32 counter can be achieved by using

a) Flip-Flop and DIV 10

b) Flip-Flop and DIV 16

c) Flip-Flop and DIV 32

d) DIV 16 and DIV 32

10. The_____input overrides the_input

a. Asynchronous, synchronous

b) Synchronous, asynchronous

c) Preset input (PRE), Clear input (CLR)

d) Clear input (CLR), Preset input (PRE)

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11. The synchronous counters are also known as Ripple Counters:

a) True

b) False

12. With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

a) 80 micro seconds

b) 8 micro seconds

c) 80 mili seconds

d) 10 micro seconds

13. Number of states in an 8-bit Johnson counter sequence are:

a) 8

b) 12

c) 14

d) 16

14. A synchronous decade counter will have___flip-flops

a) 3

b) 4

c) 7

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d) 10

15. _____is one of the examples of synchronous inputs.

a) J-K input

b) EN input

c) Preset input (PRE)

d) Clear input (CLR)

16. A decade counter is __

a) Mod-3 counter

b) Mod-5 counter

c) Mod-8 counter

d) Mod-10 counter

17. In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

a) Qt

b) 0

c) 1

d) Invalid

18. A Divide-by-20 counter can be achieved by using

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a) Flip-Flop and DIV 10

b) Flip-Flop and DIV 16

c) Flip-Flop and DIV 32

d) DIV 10 and DIV 16

19. A one-shot mono-stable device contains___

a) AND gate, Resistor, Capacitor and NOT Gate

b) NAND gate, Resistor, Capacitor and NOT Gate

c) NOR gate, Resistor, Capacitor and NOT Gate

d) XNOR gate, Resistor, Capacitor and NOT Gate

20. The_____inputs can be directly mapped to Karnaugh maps.

a) S-R

b) J-K

c) Flip-Flop

d) External

21. A mono-stable device only has a single stable state

a) True

b) False

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22. The minimum time required for the input logic levels to remain stable before the clocktransition occurs is known as the __

a) Set-up time

b) Hold time

c) Pulse interval time

d) Pulse stability time (PST)

23. The low to high or high to low transition of the clock is considered to be a(n) __

a) State

b) Edge

c) Trigger

d) One-shot

24. A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state, on the next clock pulse,to what state does the counter go?

a) 1001

b) 1011

c) 0011

d) 1100

25. When the Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of seconds.

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a) 1, 2

b) 0, 2

c) 2, 5

d) 1, 1

26. Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause theoutput to_.

a) Set

b) Toggle

c) Latch

d) Reset

27. A stage in the shift register consists of

a) A latch

b) A flip flop

c) A byte of storage

d) Four bits of storage

28. When the both inputs of edge-triggered J-K flop-flop are set to logic zero ____

a) The flop-flop is triggered

b) Q=0 and Q'=1

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c) Q=1 and Q'=0

d) The output of flip-flop remains unchanged

29. A positive edge-triggered flip-flop changes its state when _____

a) Enable input (EN) is set

b) Preset input (PRE) is set

c) Low-to-high transition of clock

d) High-to-low transition of clock

30. If a circuit suffers "Clock Skew" problem, the output of circuit can't be guaranteed.

a) True

b) False

31. The minimum time for which the input signal has to be maintained at the input of flip-flop iscalled_of the flip-flop.

a) Set-up time

b) Hold time

c) Pulse interval time

d) Pulse stability time (PST)

34. A modulus-14 counter has fourteen states requiring ____

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a) 14 flip flops

b) 14 registers

c) 4 flip flops

d) 4 registers

35. In Master-Slave flip-flop the clock signal is connected to slave flip-flop using__gate.

a) AND

b) OR

c) NOT

d) NAND

36. ___flip-flops are obsolete now.

a) Edge-triggered

b) Master-Slave

c) T-flipflop

d) D-flipflop

37. The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flipflop _____

a) Doesn't have an invalid state

b) Sets to clear when both J=0 and K=0

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c) It does not show transition on change in pulse

d) It does not accept asynchronous inputs

38. The glitches due to “Race Condition” can be avoided by using a_.

a) Gated flip-flops

b) Pulse triggered flip-flops

c) Positive-Edge triggered flip-flops

d) Negative-Edge triggered flip-flops

39. For a gated D-Latch if EN=1 and D=1 then Q(t+1) =_____

a) 0

b) 1

c) Q(t)

d) Invalid

40. ___occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

a) Race condition

b) Clock skew

c) Ripple effect

d) None of given options

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